Lenovo Global Technology

ThinkSystem SR645
3.20 GHz, AMD EPYC 74F3

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Test Date: Apr-2021
Hardware Availability: Mar-2021
Software Availability: Mar-2021

Threads

<table>
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<tr>
<th>Benchmark</th>
<th>Threads</th>
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<th>SPECspeed®2017_fp_peak</th>
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**SPEC CPU®2017 Floating Point Speed Result**

Copyright 2017-2021 Standard Performance Evaluation Corporation

**Hardware**

CPU Name: AMD EPYC 74F3
Max MHz: 4000
Nominal: 3200
Enabled: 48 cores, 2 chips
Orderable: 1.2 chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 512 KB I+D on chip per core
L3: 256 MB I+D on chip per chip, 32 MB shared / 3 cores
Other: None
Memory: 512 GB (16 x 32 GB 2Rx4 PC4-3200AA-R)
Storage: 1 x 960 GB SATA SSD
Other: None

**Software**

OS: SUSE Linux Enterprise Server 15 SP2 (x86_64)
Kernel 5.3.18-22-default
Compiler: C/C++/Fortran: Version 3.0.0 of AOCC
Parallel: Yes
Firmware: Lenovo BIOS Version D8E115E 2.01 released Mar-2021
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc: jemalloc memory allocator library v5.1.0
Power Management: BIOS set to prefer performance at the cost of additional power usage
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#### Results Table

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SPECspeed®2017_fp_base = 207
SPECspeed®2017_fp_peak = 214

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### Compiler Notes

The AMD64 AOCC Compiler Suite is available at
http://developer.amd.com/amd-aocc/

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### Submit Notes

The config file option 'submit' was used.
'numactl' was used to bind copies to the cores.
See the configuration file for details.

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### Operating System Notes

'ulimit -s unlimited' was used to set environment stack size
'ulimit -l 2097152' was used to set environment locked pages in memory limit
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
'echo 8 > /proc/sys/vm/dirty_ratio' run as root to limit dirty cache to 8% of memory.
'echo 1 > /proc/sys/vm/swappiness' run as root to limit swap usage to minimum necessary.
'echo 1 > /proc/sys/vm/zone_reclaim_mode' run as root to free node-local memory and avoid remote memory usage.
'sync; echo 3 > /proc/sys/vm/drop_caches' run as root to reset filesystem caches.
'sysctl -w kernel.randomize_va_space=0' run as root to disable address space layout randomization (ASLR) to reduce run-to-run variability.
To enable Transparent Hugepages (THP) for all allocations,
'echo always > /sys/kernel/mm/transparent_hugepage/enabled' and

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Operating System Notes (Continued)
'echo always > /sys/kernel/mm/transparent_hugepage/defrag' run as root.
To enable THP only on request for peak runs of 628.pop2_s, and 638.imagick_s,
'echo madvise > /sys/kernel/mm/transparent_hugepage/enabled' run as root.
To disable THP for peak runs of 627.cam4_s, 644.nab_s, 649.fotonik3d_s, and 654.roms_s,
'echo never > /sys/kernel/mm/transparent_hugepage/enabled' run as root.

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
GOMP_CPU_AFFINITY = "0-47"
LD_LIBRARY_PATH =
   "/home/cpu2017-1.1.5-amd-aocc300-milan-B1/amd_speed_aocc300_milan_B_lib/64;"/home/cpu2017-1.1.5-amd-aocc300-milan-B1/amd_speed_aocc300_milan_B_lib/32:" MALLOC_CONF = "retain:true"
OMP_DYNAMIC = "false"
OMP_SCHEDULE = "static"
OMP_STACKSIZE = "128M"
OMP_THREAD_LIMIT = "48"

Environment variables set by runcpu during the 619.lbm_s peak run:
GOMP_CPU_AFFINITY = "0-47"

Environment variables set by runcpu during the 654.roms_s peak run:
GOMP_CPU_AFFINITY = "0-47"

General Notes
Binaries were compiled on a system with 2x AMD EPYC 7742 CPU + 1TiB Memory using openSUSE 15.2
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

ejemalloc: configured and built with GCC v4.8.2 in RHEL 7.4 (No options specified)
ejemalloc 5.1.0 is available here:
https://github.com/jemalloc/jemalloc/releases/download/5.1.0/jemalloc-5.1.0.tar.bz2
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Platform Notes

BIOS configuration:
Operating Mode set to Maximum Performance and then set it to Custom Mode
4-Link xGMI Max Speed set to 16Gbps
SOC P-States set to P0
SMT Mode set to Disable
DLWM Support set to Disabled

Sysinfo program /home/cpu2017-1.1.5-amd-aocc300-milan-B1/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeea89d4b38e2f1c
running on localhost Tue Apr 6 06:26:33 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: AMD EPYC 74F3 24-Core Processor
  2 "physical id"s (chips)
  48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 4 5 6 8 9 10 12 13 14 16 17 18 20 21 22 24 25 26 28 29 30
physical 1: cores 0 1 2 4 5 6 8 9 10 12 13 14 16 17 18 20 21 22 24 25 26 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 48 bits physical, 48 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 2
Vendor ID: AuthenticAMD
CPU family: 25
Model: 1
Model name: AMD EPYC 74F3 24-Core Processor
Stepping: 1
CPU MHz: 2038.895
CPU max MHz: 3200.0000
CPU min MHz: 1500.0000
BogoMIPS: 6388.07
Virtualization: AMD-V

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**Platform Notes (Continued)**

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Lenovo Global Technology

ThinkSystem SR645
3.20 GHz, AMD EPYC 74F3

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

SPECspeed®2017_fp_base = 207
SPECspeed®2017_fp_peak = 214

Test Date: Apr-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Platform Notes (Continued)

VERSION="15-SP2"
VERSION_ID="15.2"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP2"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp2"

uname -a:
Linux localhost 5.3.18-22-default #1 SMP Wed Jun 3 12:16:43 UTC 2020 (720aeba) x86_64
x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB MultiHit): Not affected
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Mitigation: Speculative Store
CVE-2018-3639 (Speculative Store Bypass): Bypass disabled via prctl and
seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs
barriers and __user pointer
sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Full AMD retpoline,
IBPB: conditional, IBRS_FW, STIBP:
disabled, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected
CVE-2019-11135 (TSX Asynchronous Abort): Not affected

run-level 3 Apr 6 06:25

SPEC is set to: /home/cpu2017-1.1.5-amd-aocc300-milan-B1

From /sys/devices/virtual/dmi/id
Vendor: Lenovo
Product: ThinkSystem SR645 MB
Product Family: ThinkSystem
Serial: 1234567890

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR645
3.20 GHz, AMD EPYC 74F3

SPECspeed®2017_fp_base = 207
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CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Platform Notes (Continued)

16x Samsung M393A4K40DB3-CWE 32 GB 2 rank 3200
16x Unknown Unknown

BIOS:
- BIOS Vendor: Lenovo
- BIOS Version: D8E115E-2.01
- BIOS Date: 03/04/2021
- BIOS Revision: 2.1
- Firmware Revision: 3.1

(End of data from sysinfo program)

Compiler Version Notes

C

| 619.lbm_s(base, peak) 638.imagick_s(base, peak) 644.nab_s(base, peak) |

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

C++, C, Fortran

| 607.cactuBSSN_s(base, peak) |

AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin
AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
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Thread model: posix
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AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020_12_10) (based on LLVM Mirror.Version.12.0.0)
Target: x86_64-unknown-linux-gnu
Thread model: posix
InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

(Continued on next page)
# SPEC CPU®2017 Floating Point Speed Result

Lenovo Global Technology
ThinkSystem SR645
3.20 GHz, AMD EPYC 7F3

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## SPECspeed®2017_fp_base = 207

## SPECspeed®2017_fp_peak = 214

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### Compiler Version Notes (Continued)

**Fortran**
- 603.bwaves_s(base, peak)
- 649.fotonik3d_s(base, peak)
- 654.roms_s(base, peak)

---

**Fortran**
- 621.wrf_s(base, peak)
- 627.cam4_s(base, peak)
- 628.pop2_s(base, peak)

---

**AMD clang version 12.0.0 (CLANG: AOCC_3.0.0-Build#78 2020-12-10) (based on LLVM Mirror.Version.12.0.0)**
- Target: x86_64-unknown-linux-gnu
- Thread model: posix
- InstalledDir: /opt/AMD/aocc-compiler-3.0.0/bin

---

**Base Compiler Invocation**

**C benchmarks:**
- clang

**Fortran benchmarks:**
- flang

**Benchmarks using both Fortran and C:**
- flang clang

**Benchmarks using Fortran, C, and C++:**
- clang++ clang flang

---

### Base Portability Flags

- 603.bwaves_s: -DSPEC_LP64

---

(Continued on next page)
Base Portability Flags (Continued)

607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_CASE_FLAG -Mbyteswapio -DSPEC_LP64
627.cam4_s: -DSPEC_CASE_FLAG -DSPEC_LP64
628.pop2_s: -DSPEC_CASE_FLAG -Mbyteswapio -DSPEC_LP64
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -mno-adx -mno-sse4a -W1,-mllvm -W1,-region-vectorize
-W1,-mllvm -W1,-function-specialize
-W1,-mllvm -W1,-align-all-nofallthru-blocks=6
-W1,-mllvm -W1,-reduce-array-computations=3 -O3 -march=znver3
-fveclib=AMDLIBM -ffast-math -flto -fstruct-layout=5
-mllvm -unroll-threshold=50 -mllvm -inline-threshold=1000
-fremap-arrays -mllvm -function-specialize -flv-function-specialization
-mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
-mllvm -enable-lcm-vrp -mllvm -reduce-array-computations=3 -z muldefs
-DSPEC_OPENMP -fopenmp -fopenmp=libomp -lomp -amlb -ljemalloc
-llang -llangrti

Fortran benchmarks:
-m64 -mno-adx -mno-sse4a -W1,-mllvm -W1,-enable-X86-prefetching
-W1,-mllvm -W1,-enable-lcm-vrp -W1,-mllvm -W1,-region-vectorize
-W1,-mllvm -W1,-function-specialize
-W1,-mllvm -W1,-align-all-nofallthru-blocks=6
-W1,-mllvm -W1,-reduce-array-computations=3 -Hz,1,0x1 -O3
-march=znver3 -fveclib=AMDLIBM -ffast-math -Mrecursive
-mllvm -fuse-tile-inner-loop -funroll-loops
-mllvm -extra-vectorizer-passes -mllvm -lsr-in-nested-loop
-mllvm -enable-lcm-vrp -mllvm -reduce-array-computations=3
-mllvm -global-vectorizer-slp=true -z muldefs -DSPEC_OPENMP -fopenmp
-fopenmp=libomp -lomp -amlb -ljemalloc -llang -llangrti

Benchmarks using both Fortran and C:
-m64 -mno-adx -mno-sse4a -W1,-mllvm -W1,-enable-X86-prefetching
-W1,-mllvm -W1,-enable-lcm-vrp -W1,-mllvm -W1,-region-vectorize
-W1,-mllvm -W1,-function-specialize
-W1,-mllvm -W1,-align-all-nofallthru-blocks=6
-W1,-mllvm -W1,-reduce-array-computations=3 -O3 -march=znver3

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR645
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Tested by: Lenovo Global Technology

Base Optimization Flags (Continued):

Benchmarks using both Fortran and C (continued):
- fveclib=AMDLIBM -ffast-math -finline -fstruct-layout=5
- mllvm -unroll-threshold=50 -mllvm -inline-threshold=1000
- fremap-arrays -mllvm -function-specialize -flv-function-specialization
- mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
- mllvm -enable-licm-vrp -mllvm -reduce-array-computations=3 -Hz,1,0x1
- Mrecursive -mllvm -fuse-tile-inner-loop -funroll-loops
- mllvm -extra-vectorizer-passes -mllvm -lsr-in-nested-loop -z muldefs
- DSPEC_OPENMP -fopenmp -fopenmp=libomp -lomp -lamdlibm -ljemalloc
- lflang -lflangrti

Benchmarks using Fortran, C, and C++:
- m64 -mno-adx -mno-sse4a -std=c++98
- Wl, -mllvm -Wl, -x86-use-vzeroupper=false
- Wl, -mllvm -Wl, -region-vectorize -Wl, -mllvm -Wl, -function-specialize
- Wl, -mllvm -Wl, -align-all-nofallthru-blocks=6
- Wl, -mllvm -Wl, -reduce-array-computations=3 -O3 -march=znver3
- fveclib=AMDLIBM -ffast-math -finline -fstruct-layout=5
- mllvm -unroll-threshold=50 -mllvm -inline-threshold=1000
- fremap-arrays -mllvm -function-specialize -flv-function-specialization
- mllvm -enable-gvn-hoist -mllvm -global-vectorize-slp=true
- mllvm -enable-licm-vrp -mllvm -reduce-array-computations=3
- mllvm -enable-partial-unswitch -mllvm -unroll-threshold=100
- finline-aggressive -mllvm -loop-unschedule-threshold=200000
- mllvm -reroll-loops -mllvm -aggressive-loop-unschedule
- mllvm -extra-vectorizer-passes -mllvm -convert-pow-exp-to-int=false
- Hz,1,0x1 -Mrecursive -mllvm -fuse-tile-inner-loop -funroll-loops
- mllvm -lsr-in-nested-loop -z muldefs -DSPEC_OPENMP -fopenmp
- fopenmp=libomp -lomp -lamdlibm -ljemalloc -lflang -lflangrti

Base Other Flags

C benchmarks:
- Wno-unused-command-line-argument -Wno-return-type

Fortran benchmarks:
- Wno-unused-command-line-argument -Wno-return-type

Benchmarks using both Fortran and C:
- Wno-unused-command-line-argument -Wno-return-type

Benchmarks using Fortran, C, and C++:
- Wno-unused-command-line-argument -Wno-return-type
Lenovo Global Technology
ThinkSystem SR645
3.20 GHz, AMD EPYC 74F3

Peak Compiler Invocation

C benchmarks:  
clang

Fortran benchmarks:  
flang

Benchmarks using both Fortran and C:  
flang clang

Benchmarks using Fortran, C, and C++:  
clang++ clang flang

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

619.lbm_s: -m64 -mno-adx -mno-sse4a
- W1, -ml illum - W1, -function-specialize
- W1, -ml illum - W1, -align-all-nofallthru-blocks=6
- W1, -ml illum - W1, -reduce-array-computations=3 -Ofast
- march=znver3 -fveclib=AMDLIBM -ffast-math -flito
- fstruct-layout=5 -ml illum -unroll-threshold=50
- fremap-arrays -flv-function-specialization
- ml illum -inline-threshold=1000 -ml illum -enable-gvn-hoist
- ml illum -global-vectorize-slp=true
- ml illum -function-specialize -ml illum -enable-lcm-vrp
- ml illum -reduce-array-computations=3 -DSPEC_OPENMP -fopenmp
- fopenmp=libomp -lomp -lamdlibm -ljemalloc -lf lang

638.imagick_s: basepeak = yes

644.nab_s: basepeak = yes

Fortran benchmarks:

603.bwaves_s: basepeak = yes

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR645
3.20 GHz, AMD EPYC 74F3

SPECspeed®2017_fp_base = 207
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Test Date: Apr-2021
Hardware Availability: Apr-2021
Software Availability: Mar-2021

Peak Optimization Flags (Continued)

649.fotonik3d_s: basepeak = yes
654.roms_s: -m64 -mno-adx -mno-sse4a
-Wl,-mlllvm -Wl,-enable-X86-prefetching
-Wl,-mlllvm -Wl,-enable-licm-vrp
-Wl,-mlllvm -Wl,-function-specialize
-Wl,-mlllvm -Wl,-align-all-nofallthru-blocks=6
-Wl,-mlllvm -Wl,-reduce-array-computations=3 -Ofast
-march=znver3 -fveclib=AMDLIBM -ffast-math -Mrecursive
-mlllvm -reduce-array-computations=3
-mlllvm -global-vectorize-slp=true -mlllvm -enable-licm-vrp
-DSPEC_OPENMP -fopenmp -fopenmp=libomp -lomp -lamdlibm
-ljemalloc -lflang

Benchmarks using both Fortran and C:
621.wrf_s: basepeak = yes
627.cam4_s: basepeak = yes
628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:
607.cactuBSSN_s: basepeak = yes

Peak Other Flags

C benchmarks:
-Wno-unused-command-line-argument -Wno-return-type

Fortran benchmarks:
-Wno-unused-command-line-argument -Wno-return-type

Benchmarks using both Fortran and C:
-Wno-unused-command-line-argument -Wno-return-type

Benchmarks using Fortran, C, and C++:
-Wno-unused-command-line-argument -Wno-return-type

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-Milan-D.html
## Lenovo Global Technology

### SPEC CPU®2017 Floating Point Speed Result

**Tested by:** Lenovo Global Technology  
**Test Sponsor:** Lenovo Global Technology  

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- **CPU2017 License:** 9017  
- **Test Date:** Apr-2021  
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You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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