SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyron Camarero DS400E1U-224R4
(2.50 GHz, Intel Xeon Gold 6248)

SPECrates®2017_fp_base = 239
SPECrates®2017_fp_peak = 242

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Hardware
CPU Name: Intel Xeon Gold 6248
Max MHz: 3900
Nominal: 2500
Enabled: 40 cores, 2 chips, 2 threads/core
Orderable: 1,2 (chip)s
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 27.5 MB I+D on chip per chip
Other: None
Memory: 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R)
Storage: 1 x 480 GB SATA SSD
Other: None

Software
OS: CentOS Linux release 8.3.2011
Compiler: C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux;
Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux
Parallel: No
Firmware: Version 3.4 released Oct-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: jemalloc memory allocator V5.0.1
Power Management: BIOS set to prefer performance at the cost of additional power usage
**SPEC CPU®2017 Floating Point Rate Result**

**Tyrone Systems**  
(Test Sponsor: Netweb Pte Ltd)  
Tyrone Camarero DS400E1U-224R4  
(2.50 GHz, Intel Xeon Gold 6248)  

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>80</td>
<td>1611</td>
<td>498</td>
<td>1614</td>
<td>497</td>
<td>1611</td>
<td>498</td>
<td></td>
<td>80</td>
<td>1611</td>
<td>498</td>
<td>1611</td>
<td>498</td>
<td></td>
<td>80</td>
<td>1611</td>
<td>498</td>
<td>1611</td>
<td>498</td>
<td>1612</td>
<td>498</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>80</td>
<td>304</td>
<td>333</td>
<td>304</td>
<td>333</td>
<td>306</td>
<td>331</td>
<td></td>
<td>80</td>
<td>304</td>
<td>333</td>
<td>304</td>
<td>333</td>
<td></td>
<td>80</td>
<td>304</td>
<td>333</td>
<td>306</td>
<td>331</td>
<td></td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td>80</td>
<td>404</td>
<td>188</td>
<td>406</td>
<td>187</td>
<td>404</td>
<td>188</td>
<td></td>
<td>80</td>
<td>404</td>
<td>188</td>
<td>404</td>
<td>188</td>
<td></td>
<td>80</td>
<td>404</td>
<td>188</td>
<td>406</td>
<td>187</td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>80</td>
<td>1643</td>
<td>127</td>
<td>1646</td>
<td>127</td>
<td>1644</td>
<td>127</td>
<td></td>
<td>80</td>
<td>1643</td>
<td>127</td>
<td>1642</td>
<td>127</td>
<td></td>
<td>80</td>
<td>1643</td>
<td>127</td>
<td>1642</td>
<td>127</td>
<td>1642</td>
<td>127</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>80</td>
<td>653</td>
<td>286</td>
<td>649</td>
<td>288</td>
<td>649</td>
<td>288</td>
<td></td>
<td>80</td>
<td>564</td>
<td>331</td>
<td>559</td>
<td>334</td>
<td></td>
<td>564</td>
<td>331</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>80</td>
<td>721</td>
<td>117</td>
<td>721</td>
<td>117</td>
<td>721</td>
<td>117</td>
<td></td>
<td>80</td>
<td>721</td>
<td>117</td>
<td>721</td>
<td>117</td>
<td></td>
<td>721</td>
<td>117</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>80</td>
<td>840</td>
<td>213</td>
<td>846</td>
<td>212</td>
<td>840</td>
<td>213</td>
<td></td>
<td>80</td>
<td>818</td>
<td>219</td>
<td>811</td>
<td>221</td>
<td></td>
<td>818</td>
<td>219</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>526.blender_r</td>
<td>80</td>
<td>490</td>
<td>249</td>
<td>489</td>
<td>249</td>
<td>490</td>
<td>249</td>
<td></td>
<td>80</td>
<td>490</td>
<td>249</td>
<td>489</td>
<td>249</td>
<td></td>
<td>490</td>
<td>249</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>80</td>
<td>525</td>
<td>267</td>
<td>526</td>
<td>267</td>
<td>526</td>
<td>267</td>
<td></td>
<td>80</td>
<td>525</td>
<td>267</td>
<td>525</td>
<td>267</td>
<td></td>
<td>528</td>
<td>265</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>80</td>
<td>289</td>
<td>688</td>
<td>289</td>
<td>689</td>
<td>288</td>
<td>691</td>
<td></td>
<td>80</td>
<td>289</td>
<td>688</td>
<td>289</td>
<td>689</td>
<td></td>
<td>289</td>
<td>689</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>544.nab_r</td>
<td>80</td>
<td>315</td>
<td>427</td>
<td>319</td>
<td>422</td>
<td>318</td>
<td>424</td>
<td></td>
<td>80</td>
<td>315</td>
<td>427</td>
<td>319</td>
<td>422</td>
<td></td>
<td>318</td>
<td>424</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>80</td>
<td>2045</td>
<td>152</td>
<td>2040</td>
<td>153</td>
<td>2043</td>
<td>153</td>
<td></td>
<td>80</td>
<td>2045</td>
<td>152</td>
<td>2040</td>
<td>153</td>
<td></td>
<td>2043</td>
<td>153</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>80</td>
<td>1320</td>
<td>96.3</td>
<td>1320</td>
<td>96.3</td>
<td>1324</td>
<td>96.0</td>
<td></td>
<td>80</td>
<td>1326</td>
<td>95.9</td>
<td>1324</td>
<td>96.0</td>
<td>1322</td>
<td>96.1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Compiler Notes**

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.

The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"

MALLOC_CONF = "retain:true"
SUN SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.50 GHz, Intel Xeon Gold 6248)

SPECrate®2017_fp_base = 239
SPECrate®2017_fp_peak = 242

General Notes

Binaries compiled on a system with 2x Intel Cascade Lake CPU + 384 GB RAM memory using Centos 8.2 x86_64
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation built with the Centos 8.2 x86_64, and the system compiler gcc 4.8.5 sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases

Platform Notes

BIOS Settings:
Power Technology = Custom
Power Performance Tuning = BIOS Controls EPB
ENERGY_PERF_BIAS_CFG mode = Extreme Performance
SNC = Enable
Stale AtoS = Disable
IMC Interleaving = 1-way Interleave
Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6538 of 2020-09-24 e8664e66d2d7080afeaa89d4b38e2f1c
running on spec Wed Feb 3 20:33:03 2021

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

Page 3
Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
Stepping: 7
CPU MHz: 3199.990
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56
NUMA node1 CPU(s): 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
NUMA node2 CPU(s): 20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76
NUMA node3 CPU(s): 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref pni pclmulqdq dts64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdseed rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_13 invpcid_single intel_pmm ssbd mba ibrs ibpb stibp ibrs_enhanced fsagent tsc_adjust bmi1 hle avx2 smep bmi2 64bit threading base tsc_adjust bmi1 hle avx2 smep bmi2 64bit threading base tsc_adjust bmi1 hle avx2
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.50 GHz, Intel Xeon Gold 6248)

SPECrG®2017_fp_base = 239
SPECrG®2017_fp_peak = 242

Copyright 2017-2021 Standard Performance Evaluation Corporation

Available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
node 0 size: 90298 MB
node 0 free: 84805 MB
node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
node 1 size: 92391 MB
node 1 free: 88010 MB
node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
node 2 size: 92199 MB
node 2 free: 88045 MB
node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
node 3 size: 92036 MB
node 3 free: 88079 MB

node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 394858824 kB
HugePages_Total: 0
Hugepagesize: 2048 kB
/sbin/tuned-adm active
    Current active profile: throughput-performance
/sys/devices/system/cpu/cpu*/cpufreq/scaling_governor has performance

From /etc/*release*/etc/*version*
centos-release: CentOS Linux release 8.3.2011
centos-release-upstream: Derived from Red Hat Enterprise Linux 8.3
os-release:  
    NAME="CentOS Linux"
    VERSION="8"
    ID="centos"
    ID_LIKE="rhel fedora"
    VERSION_ID="8"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="CentOS Linux 8"
    ANSI_COLOR="#0;31"
redhat-release: CentOS Linux release 8.3.2011
system-release: CentOS Linux release 8.3.2011
system-release-cpe: cpe:/o:centos:centos:8

(Continued on next page)
SPECCPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.50 GHz, Intel Xeon Gold 6248)

SPECraten®2017_fp_base = 239
SPECraten®2017_fp_peak = 242

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Test Date: Feb-2021
Hardware Availability: Aug-2020
Software Availability: Dec-2020

Platform Notes (Continued)

uname -a:
    Linux spec 4.18.0-240.el8.x86_64 #1 SMP Fri Sep 25 19:48:47 UTC 2020 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-12207 (iTLB Multi-hit): KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitation
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
CVE-2020-0543 (Special Register Buffer Data Sampling): Not affected

run-level 3 Feb 3 12:31

SPEC is set to: /home/cpu2017
    Filesystem     Type  Size  Used Avail Use% Mounted on
    /dev/mapper/cl-home xfs   372G  156G  216G  42% /home

From /sys/devices/virtual/dmi/id
    Vendor:         Tyrone Systems
    Product:        Tyrone Camarero DS400E1
    Serial:         S263875X9527668

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMI BIOS" standard.

Memory:
    12x NO DIMM NO DIMM
    12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

BIOS:
    BIOS Vendor:      American Megatrends Inc.
    BIOS Version:    3.4
    BIOS Date:       10/30/2020
    BIOS Revision:   5.14

(End of data from sysinfo program)

(Continued on next page)
Platform Notes (Continued)

Sysinfo incorrectly parsed dmidecode output. Configured memory speed is 2933.

Compiler Version Notes

-------------------------------------------------------------------------------
| C    | 519.libm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |
|      |                                                                          |
| Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1  |
| NextGen Build 20200304                                                      |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.             |
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
| C++   | 508.namd_r(base, peak) 510.parest_r(base, peak)                         |
|       |                                                                          |
| Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1|
| NextGen Build 20200304                                                      |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.             |
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
| C++, C | 511.povray_r(base) 526.blender_r(base, peak)                           |
|        |                                                                          |
| Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1|
| NextGen Build 20200304                                                      |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.             |
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
| C++, C | 511.povray_r(peak)                                                  |
|        |                                                                          |
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,|
|        | Version 19.1.1.217 Build 20200306                                    |
|         | Copyright (C) 1985-2020 Intel Corporation. All rights reserved.        |
-------------------------------------------------------------------------------

-------------------------------------------------------------------------------
| C++, C | 511.povray_r(base) 526.blender_r(base, peak)                         |
|        |                                                                          |
| Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1|
| NextGen Build 20200304                                                      |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.             |
-------------------------------------------------------------------------------

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.50 GHz, Intel Xeon Gold 6248)

SPECrater®2017_fp_base = 239
SPECrater®2017_fp_peak = 242

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Compiler Version Notes (Continued)

Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------
C++, C          | 511.povray_r(peak)
------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------
Fortran          | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                                                                             554.roms_r(base, peak)
------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------
Fortran, C       | 521.wrf_r(base) 527.cam4_r(base, peak)
------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306

(Continued on next page)
Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.50 GHz, Intel Xeon Gold 6248)

SPECrater®2017_fp_base = 239
SPECrater®2017_fp_peak = 242

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Compiler Version Notes (Continued)
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
---------------------------------------------------------------------
Fortran, C          | 521.wrf_r(peak)
Intel (R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) C Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
---------------------------------------------------------------------
Fortran, C          | 521.wrf_r(base) 527.cam4_r(base, peak)
Intel (R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
---------------------------------------------------------------------
Fortran, C          | 521.wrf_r(peak)
Intel (R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel (R) C Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks: icc
C++ benchmarks: icpc

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.50 GHz, Intel Xeon Gold 6248)

SPECrate®2017_fp_base = 239
SPECrate®2017_fp_peak = 242

<table>
<thead>
<tr>
<th>CPU2017 License: 006042</th>
<th>Test Date: Feb-2021</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Netweb Pte Ltd</td>
<td>Hardware Availability: Aug-2020</td>
</tr>
<tr>
<td>Tested by: Tyrone Systems</td>
<td>Software Availability: Dec-2020</td>
</tr>
</tbody>
</table>

Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.llvm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
-ljemalloc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2021 Standard Performance Evaluation Corporation

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.50 GHz, Intel Xeon Gold 6248)

SPECrate®2017_fp_base = 239
SPECrate®2017_fp_peak = 242

CPU2017 License: 006042
Test Sponsor: Netweb Pte Ltd
Tested by: Tyrone Systems

Base Optimization Flags (Continued)

C++ benchmarks (continued):
- mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
- L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
- m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- fuse=ld.gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
- ffinitenumber-only -qopt-multiple-gather-scatter-by-shuffles
- qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
- auto -mbranches-within-32B-boundaries -L/usr/local/je5.0.1-64/lib
  -ljemalloc

Benchmarks using both Fortran and C:
- m64 -qnextgen -std=c11
- Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- fuse=ld.gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
- qopt-prefetch -ffinitenumber-only
- qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
- align array32byte -auto -mbranches-within-32B-boundaries
- L/usr/local/je5.0.1-64/lib -ljemalloc

Benchmarks using both C and C++:
- m64 -qnextgen -std=c11
- Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- fuse=ld.gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib
- ljemalloc

Benchmarks using Fortran, C, and C++:
- m64 -qnextgen -std=c11
- Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
- fuse=ld.gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
- funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
- qopt-prefetch -ffinitenumber-only
- qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
- align array32byte -auto -mbranches-within-32B-boundaries
- L/usr/local/je5.0.1-64/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc

(Continued on next page)
Peak Compiler Invocation (Continued)

C++ benchmarks:
  icpc

Fortran benchmarks:
  ifort

Benchmarks using both Fortran and C:
  ifort icc

Benchmarks using both C and C++:
  icpc icc

Benchmarks using Fortran, C, and C++:
  icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.1bm_r: basepeak = yes
538.imagick_r: basepeak = yes
544.nab_r: basepeak = yes

C++ benchmarks:

508.namd_r: basepeak = yes
510.parest_r: -m64 -qnextgen -W1,-plugin-opt=-x86-branches-within-32B-boundaries -W1,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:

(Continued on next page)
Peak Optimization Flags (Continued)

503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto
-L/usr/local/je5.0.1-64/lib -ljemalloc

527.cam4_r: basepeak = yes

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/je5.0.1-64/lib -ljemalloc

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/Tyrone-Platform-Settings-V1.2-CLX-revB.xml
SPEC CPU®2017 Floating Point Rate Result

Tyrone Systems
(Test Sponsor: Netweb Pte Ltd)
Tyrone Camarero DS400E1U-224R4
(2.50 GHz, Intel Xeon Gold 6248)

**SPECrate®2017_fp_base = 239**
**SPECrate®2017_fp_peak = 242**

<table>
<thead>
<tr>
<th>Test Sponsor:</th>
<th>Netweb Pte Ltd</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tested by:</td>
<td>Tyrone Systems</td>
</tr>
<tr>
<td>CPU2017 License:</td>
<td>006042</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Feb-2021</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2020</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Dec-2020</td>
</tr>
</tbody>
</table>

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.5 on 2021-02-03 10:03:02-0500.
Report generated on 2021-03-02 15:50:14 by CPU2017 PDF formatter v6255.
Originally published on 2021-03-02.