## SPEC CPU® 2017 Integer Rate Result

**New H3C Technologies Co., Ltd.**

**H3C UniServer R4900 G3 (Intel Xeon Silver 4210R)**

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- **CPU2017 License**: 9066
- **Test Sponsor**: New H3C Technologies Co., Ltd.
- **Tested by**: New H3C Technologies Co., Ltd.
- **Test Date**: Oct-2020
- **Hardware Availability**: Mar-2020
- **Software Availability**: Apr-2020

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### CPU Specifications

- **CPU Name**: Intel Xeon Silver 4210R
- **Max MHz**: 3200
- **Nominal**: 2400
- **Enabled**: 20 cores, 2 chips, 2 threads/core
- **Orderable**: 1.2 chips
- **Cache L1**: 32 KB I + 32 KB D on chip per core
- **L2**: 1 MB I+D on chip per core
- **L3**: 13.75 MB I+D on chip per chip
- **Other**: None
- **Memory**: 192 GB (12 x 16 GB 2Rx8 PC4-2933V-R, running at 2400)
- **Storage**: 2 x 600 GB SAS HDD, 10000RPM, RAID 1
- **Other**: None

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| Peak              |        |         |       |         |       |         |       |
|                   |        |         |       |         |       |         |       |
| Base              |        |         |       |         |       |         |       |
| 500.perlbench_r   | 40     | 645     | 98.8  | 642     | 99.1  | 642     | 99.2  |
| 502.gcc_r         | 40     | 538     | 105   | 536     | 106   | 537     | 106   |
| 505.mcf_r         | 40     | 318     | 204   | 319     | 203   | 319     | 203   |
| 520.omnetpp_r     | 40     | 705     | 105   | 710     | 73.9  | 704     | 74.5  |
| 523.xalancbmk_r   | 40     | 264     | 160   | 262     | 161   | 262     | 161   |
| 525.x264_r        | 40     | 262     | 160   | 262     | 258   | 271     | 258   |
| 531.deepsjeng_r   | 40     | 466     | 98.3  | 466     | 98.5  | 467     | 98.1  |
| 541.leela_r       | 40     | 715     | 92.6  | 718     | 92.3  | 715     | 92.6  |
| 548.exchange2_r   | 40     | 446     | 235   | 445     | 236   | 444     | 236   |
| 557.xz_r          | 40     | 605     | 71.4  | 602     | 71.7  | 602     | 71.8  |

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux. The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
/home/speccpu/lib/intel64:/home/speccpu/lib/ia32:/home/speccpu/je5.0.1-32

MALLOC_CONF = "retain:true"
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**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
 sync; echo 3>/proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

jemalloc, a general purpose malloc implementation

built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5


---

**Platform Notes**

BIOS settings:
Set SNC to Enabled
Set IMC Interleaving to 1-way Interleave
Set Patrol Scrub to Disabled

Sysinfo program /home/speccpu/bin/sysinfo

Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
running on localhost.localdomain Thu Oct 22 10:58:30 2020

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see

https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
2 "physical id"s (chips)
40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
```

From lscpu:

```
Architecture: x86_64
```

(Continued on next page)
### Platform Notes (Continued)

- **CPU op-mode(s):** 32-bit, 64-bit
- **Byte Order:** Little Endian
- **CPU(s):** 40
- **On-line CPU(s) list:** 0-39
- **Thread(s) per core:** 2
- **Core(s) per socket:** 10
- **Socket(s):** 2
- **NUMA node(s):** 2
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
- **Stepping:** 7
- **CPU MHz:** 2629.298
- **CPU max MHz:** 3200.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 4800.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 14080K
- **NUMA node0 CPU(s):** 0-9, 20-29
- **NUMA node1 CPU(s):** 10-19, 30-39
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt pppct_prepare tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pdpin ssbd mba ibpb stibp ibrs enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invvpidd rtm cmn mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xgetbv1 xsavec xsaveopt xsaves cqm_llc cqm_occuup_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pkup ospke avx512_vnni md_clear flush_l1d arch_capabilities

```
/cache.data
    cache size : 14080 KB
```

From `numactl --hardware` WARNING: a numactl 'node' might or might not correspond to a physical chip.
- **available:** 2 nodes (0-1)
  - node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
  - node 0 size: 96019 MB
  - node 0 free: 94764 MB
  - node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39

(Continued on next page)
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Platform Notes (Continued)

node 1 size: 96735 MB
node 1 free: 95948 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 197381372 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
   os-release:
      NAME="Red Hat Enterprise Linux"
      VERSION="8.2 (Ootpa)"
      ID="rhel"
      ID_LIKE="fedora"
      VERSION_ID="8.2"
      PLATFORM_ID="platform:el8"
      PRETTY_NAME="Red Hat Enterprise Linux 8.2 (Ootpa)"
      ANSI_COLOR="0;31"
   redhat-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
   system-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
   system-release-cpe: cpe:/o:redhat:enterprise_linux:8.2:ga

uname -a:
Linux localhost.localdomain 4.18.0-193.el8.x86_64 #1 SMP Fri Mar 27 14:35:58 UTC 2020
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

itlb_multihit: KVM: Mitigation: Split huge pages
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swaps barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
tsx_async_abort: Mitigation: Clear CPU buffers; SMT vulnerable

run-level 3 Oct 22 10:52

SPEC is set to: /home/speccpu

(Continued on next page)
New H3C Technologies Co., Ltd.  
H3C UniServer R4900 G3 (Intel Xeon Silver 4210R)

SPECrate®2017_int_base = 122  
SPECrate®2017_int_peak = 126

CPU2017 License: 9066  
Test Sponsor: New H3C Technologies Co., Ltd.  
Tested by: New H3C Technologies Co., Ltd.

Test Date: Oct-2020  
Hardware Availability: Mar-2020  
Software Availability: Apr-2020

Platform Notes (Continued)

Filesystem  Type  Size  Used  Avail  Use%  Mounted on
/dev/mapper/rhel-home  xfs  503G  25G  478G  5%  /home

From /sys/devices/virtual/dmi/id
BIOS: American Megatrends Inc. 2.00.33 08/22/2019
Vendor: H3C
Product: RS33M2C9S
Product Family: Rack

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
12x NO DIMM NO DIMM
12x Samsung M393A2K43CB2-CVF 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

----------------------------------------
C | 502.gcc_r(peak)
----------------------------------------
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

----------------------------------------
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base)
----------------------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

----------------------------------------
C | 500.perlbench_r(peak) 557.xz_r(peak)
----------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
New H3C Technologies Co., Ltd.
H3C UniServer R4900 G3 (Intel Xeon Silver 4210R)

SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 122
SPECrate®2017_int_peak = 126

CPU2017 License: 9066
Test Sponsor: New H3C Technologies Co., Ltd.
Test Date: Oct-2020
Tested by: New H3C Technologies Co., Ltd.
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Compiler Version Notes (Continued)

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H3C UniServer R4900 G3 (Intel Xeon Silver 4210R)

SPEC CPU®2017 Integer Rate Result

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Hardware Availability: Mar-2020
Software Availability: Apr-2020

Compiler Version Notes (Continued)

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------------------------------------------------------------------------------
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
        | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
### Base Optimization Flags

**C benchmarks:**
- `-m64` `-qnextgen` `-std=c11`
- `-Wl,-plugin-opt=-x86-branches-within-32B-boundaries` `-Wl,-z,muldefs`
- `-xCORE-AVX512` `-O3` `-ffast-math` `-flto` `-mfpmath=sse` `-funroll-loops`
- `-fuse-ld=gold` `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

**C++ benchmarks:**
- `-m64` `-qnextgen` `-Wl,-plugin-opt=-x86-branches-within-32B-boundaries`
- `-Wl,-z,muldefs` `-xCORE-AVX512` `-O3` `-ffast-math` `-flto` `-mfpmath=sse`
- `-funroll-loops` `-fuse-ld=gold` `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

**Fortran benchmarks:**
- `-m64` `-Wl,-plugin-opt=-x86-branches-within-32B-boundaries` `-Wl,-z,muldefs`
- `-xCORE-AVX512` `-O3` `-ipo` `-no-prec-div` `-qopt-mem-layout-trans=4`
- `-nostandard-realloc-lhs` `-align array32byte` `-auto`
- `-mbranches-within-32B-boundaries`
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin`
- `-lqkmalloc`

---

### Peak Compiler Invocation

**C benchmarks:**
- `icc`

**C++ benchmarks:**
- `icpc`

**Fortran benchmarks:**
- `ifort`

---

### Peak Portability Flags

- `500.perlbmk_r: -DSPEC_LP64 -DSPEC_LINUX_X64`
- `502.gcc_r: -D_FILE_OFFSET_BITS=64`
- `505.mcf_r: -DSPEC(LP64`
- `520.omnetpp_r: -DSPEC(LP64`
- `523.xalancbmk_r: -DSPEC(LP64 -DSPEC_LINUX`

*(Continued on next page)*
New H3C Technologies Co., Ltd.
H3C UniServer R4900 G3 (Intel Xeon Silver 4210R)

SPECrate®2017_int_base = 122
SPECrate®2017_int_peak = 126

Peak Portability Flags (Continued)

525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

502.gcc_r: -m32
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/ia32_lin
-std=gnu89
- Wl,-plugin-opt=-x86-branches-within-32B-boundaries
- Wl,-z,muldefs -fprofile-generate(pass 1)
 -fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
 -Ofast(pass 1) -O3 -ffast-math -qnextgen -fuse-ld=gold
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc32-5.0.1/lib
-ljemalloc

505.mcf_r: basepeak = yes

525.x264_r: -m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -flto -O3 -ffast-math
-fuse-ld=gold -qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:

(Continued on next page)
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Peak Optimization Flags (Continued)

520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:
548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/New_H3C-Platform-Settings-V1.4-CLX-RevB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1l-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/New_H3C-Platform-Settings-V1.4-CLX-RevB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-10-21 22:58:29-0400.