**SPEC CPU®2017 Floating Point Speed Result**

New H3C Technologies Co., Ltd.  
H3C UniServer R4900 G3 (Intel Xeon Silver 4210R)

<table>
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<tr>
<th>SPECspeed®2017_fp_base</th>
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<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>80.2</td>
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**CPU2017 License:** 9066  
**Test Sponsor:** New H3C Technologies Co., Ltd.  
**Tested by:** New H3C Technologies Co., Ltd.

**Threads**

<table>
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<tr>
<th>Benchmark</th>
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<tr>
<td>603.bwaves_s</td>
<td>20</td>
<td>345</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>20</td>
<td>91.5</td>
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<tr>
<td>619.lbm_s</td>
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<tr>
<td>621.wrf_s</td>
<td>20</td>
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<tr>
<td>627.cam4_s</td>
<td>20</td>
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<td>20</td>
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<tr>
<td>644.nab_s</td>
<td>20</td>
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</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>20</td>
<td>64.1</td>
<td></td>
</tr>
<tr>
<td>654.roms_s</td>
<td>20</td>
<td>71.5</td>
<td></td>
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**Hardware**

- **CPU Name:** Intel Xeon Silver 4210R  
- **Max MHz:** 3200  
- **Nominal:** 2400  
- **Enabled:** 20 cores, 2 chips  
- **Orderable:** 1.2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 13.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 192 GB (12 x 16 GB 2Rx8 PC4-2933V-R, running at 2400)  
- **Storage:** 2 x 600 GB SAS HDD, 10000RPM, RAID 1  
- **Other:** None

**Software**

- **OS:** Red Hat Enterprise Linux release 8.2 (Ootpa)  
  4.18.0-193.el8.x86_64  
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler Build 20200306 for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler Build 20200306 for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 2.00.33 released Aug-2019 BIOS  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
New H3C Technologies Co., Ltd.  
H3C UniServer R4900 G3 (Intel Xeon Silver 4210R)

SPECspeed®2017_fp_base = 79.4
SPECspeed®2017_fp_peak = 80.2

Results Table

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<th>Seconds</th>
<th>Ratio</th>
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<td>71.4</td>
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SPECspeed®2017_fp_base = 79.4  
SPECspeed®2017_fp_peak = 80.2

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/speccpu/lib/intel64:/home/speccpu/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Files sistem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

(Continued on next page)
SPEC CPU®2017 Floating Point Speed Result

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CPU2017 License: 9066
Test Sponsor: New H3C Technologies Co., Ltd.
Tested by: New H3C Technologies Co., Ltd.
Test Date: Oct-2020
Hardware Availability: Mar-2020
Software Availability: Apr-2020

General Notes (Continued)

Platform Notes

BIOS Settings:
Set Hyper Threading to Disabled
Set IMC Interleaving to 2-way Interleave

Sysinfo program /home/speccpu/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eddb1e6e46a485a0011
running on localhost.localdomain Thu Oct 22 04:20:52 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
 2 "physical id"s (chips)
 20 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 10
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 234 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 20
On-line CPU(s) list: 0-19
Thread(s) per core: 1
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 2875.883
CPU max MHZ: 3200.0000
CPU min MHZ: 1000.0000
BogoMIPS: 4800.00

(Continued on next page)
SPEC CPU®2017 Floating Point Speed Result

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Platform Notes (Continued)

Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9
NUMA node1 CPU(s): 10-19
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pmm ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xSAVE xXSAVEC xSAVEOPT cqm_llc cqm_mbb_local dtherm ida arat pfn pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

/proc/cpuinfo cache data

cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9
node 0 size: 95050 MB
node 0 free: 93143 MB
node 1 cpus: 10 11 12 13 14 15 16 17 18 19
node 1 size: 96765 MB
node 1 free: 89955 MB
node distances:

node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 196418676 KB
HugePages_Total: 0
Hugepagesize: 2048 KB

From /etc/*release*/etc/*version*
os-release:
NAME="Red Hat Enterprise Linux"
VERSION="8.2 (Ootpa)"
ID="rhel"

(Continued on next page)
New H3C Technologies Co., Ltd.  

H3C UniServer R4900 G3 (Intel Xeon Silver 4210R)  

**SPECspeed®2017_fp_base = 79.4**  
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---

**Platform Notes (Continued)**

```ini
ID_LIKE="fedora"
VERSION_ID="8.2"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.2 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.2 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.2:ga
```

uname -a:
```
Linux localhost.localdomain 4.18.0-193.el8.x86_64 #1 SMP Fri Mar 27 14:35:58 UTC 2020
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **itlb_multihit:** KVM: Mitigation: Split huge pages
- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
- **tsx_async_abort:** Mitigation: Clear CPU buffers; SMT disabled

run-level 3 Oct 21 22:59

SPEC is set to: /home/speccpu
```
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 503G 18G 485G 4% /home
```

From /sys/devices/virtual/dmi/id
```
BIOS: American Megatrends Inc. 2.00.33 08/22/2019
Vendor: H3C
Product: RS33M2C9S
Product Family: Rack
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

**Memory:**
```
12x NO DIMM NO DIMM
12x Samsung M393A2K43CB2-CVF 16 GB 2 rank 2933
```

(Continued on next page)
New H3C Technologies Co., Ltd. | SPECspeed®2017_fp_base = 79.4
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Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

C

619.lbm_s(base, peak) 638.imagick_s(base, peak)
644.nab_s(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++, C, Fortran | 607.cactuBSSN_s(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran

603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
654.roms_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran, C

621.wrf_s(base, peak) 627.cam4_s(base, peak)
628.pop2_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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**Compiler Version Notes (Continued)**

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**Base Compiler Invocation**

C benchmarks:

`icc`

Fortran benchmarks:

`ifort`

Benchmarks using both Fortran and C:

`ifort icc`

Benchmarks using Fortran, C, and C++:

`icpc icc ifort`

---

**Base Portability Flags**

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

---

**Base Optimization Flags**

C benchmarks:

-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

Fortran benchmarks:

-m64 -Wl,-z,nowdefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs

(Continued on next page)
## New H3C Technologies Co., Ltd.

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### Base Optimization Flags (Continued)

Fortran benchmarks (continued):
- `mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/lib` 
- `ljemalloc`

Benchmarks using both Fortran and C:
- `m64 -std=c11 -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div` 
- `qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp` 
- `DSPC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs` 
- `L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

Benchmarks using Fortran, C, and C++:
- `m64 -std=c11 -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div` 
- `qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp` 
- `DSPC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs` 
- `L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

### Peak Compiler Invocation

C benchmarks:
- `icc`

Fortran benchmarks:
- `ifort`

Benchmarks using both Fortran and C:
- `ifort icc`

Benchmarks using Fortran, C, and C++:
- `icpc icc ifort`

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

C benchmarks:
- `619.lbm_s: basepeak = yes`

(Continued on next page)
### Peak Optimization Flags (Continued)

638.imagick_s: basepeak = yes

644.nab_s: -m64 -std=c11 -Wl,-z,muldefs -xcORE-AVX512 -ipo -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:

603.bwaves_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xcORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -qopenmp -nstandard-realloc-lhs
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)
-prof-use(pass 2) -ipo -xcORE-AVX512 -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nstandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

627.cam4_s: basepeak = yes

628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:

607.cactuBSSN_s: basepeak = yes

---

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/New_H3C-Platform-Settings-V1.4-CLX-RevB.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml
http://www.spec.org/cpu2017/flags/New_H3C-Platform-Settings-V1.4-CLX-RevB.xml
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</tr>
</tbody>
</table>

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