# SPEC CPU® 2017 Floating Point Speed Result

## Supermicro

SuperStorage 6029P-E1CR24H  
(X11DSC+, Intel Xeon Silver 4215R)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
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</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>77.3</td>
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</tbody>
</table>

**CPU2017 License:** 001176  
**Test Sponsor:** Supermicro  
**Tested by:** Supermicro

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### Hardware

- **CPU Name:** Intel Xeon Silver 4215R  
- **Max MHz:** 4000  
- **Nominal:** 3200  
- **Enabled:** 16 cores, 2 chips  
- **Orderable:** 1.2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 11 MB I+D on chip per core  
- **Other:** None  
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R)  
- **Storage:** 1 x 200 GB SATA III SSD  
- **Other:** None

### Software

- **OS:** Red Hat Enterprise Linux release 8.1  
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux
- **Parallel:** Yes  
- **Firmware:** Version 3.2 released Oct-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage

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<tr>
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The table below shows the SPEC CPU 2017 Floating Point Speed Results for the Supermicro SuperStorage 6029P-E1CR24H configuration.

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<tr>
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<tr>
<td>607.cactuBSSN_s</td>
<td>16</td>
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<td>619.lbm_s</td>
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*Copyright 2017-2020 Standard Performance Evaluation Corporation*  
*https://www.spec.org/*
SPEC CPU®2017 Floating Point Speed Result

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Supermicro
SuperStorage 6029P-E1CR24H
(X11DSC+, Intel Xeon Silver 4215R)

CPU2017 License: 001176
Test Sponsor: Supermicro
Tested by: Supermicro

SPECspeed®2017_fp_base = 76.3
SPECspeed®2017_fp_peak = 77.3

Results Table

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<th>Seconds</th>
<th>Ratio</th>
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SPECspeed®2017_fp_base = 76.3
SPECspeed®2017_fp_peak = 77.3

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux. The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain=true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

sync; echo 3>/proc/sys/vm/drop_caches

(Continued on next page)
**Supermicro**

SuperStorage 6029P-E1CR24H  
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**SPECspeed®2017_fp_base** = 76.3  
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---

**General Notes (Continued)**

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.


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**Platform Notes**

BIOS Settings:
- Power Technology = Custom
- Power Performance Tuning = BIOS Controls EPB
- ENERGY_PERF_BIAS_CFG mode = Performance
- Hyper-Threading = Disable
- Stale AtoS = Disable
- Patrol Scrub = Disable

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
running on RHEL81-01 Tue Sep 8 06:23:17 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name: Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
  - 2 "physical id"s (chips)
  - 16 "processors"
  - cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    - cpu cores: 8
    - siblings: 8
    - physical 0: cores 0 1 2 3 4 5 6 7
    - physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 16
- On-line CPU(s) list: 0-15
- Thread(s) per core: 1

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(Continued on next page)
Platform Notes (Continued)

Core(s) per socket:  8
Socket(s):           2
NUMA node(s):       2
Vendor ID:          GenuineIntel
CPU family:         6
Model:              85
Model name:         Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
Stepping:           7
CPU MHz:            999.999
BogoMIPS:           6400.00
Virtualization:     VT-x
L1d cache:          32K
L1i cache:          32K
L2 cache:           1024K
L3 cache:           11264K
NUMA node0 CPU(s):  0-7
NUMA node1 CPU(s):  8-15
Flags:              fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnummi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2  8 ept pti msram invpcid rtm cqm mpx rdod_a avx512fs rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512v1 xsavesopt xsaveopt xsavec xgetbv1 xsavec qcm_llc qcm_occup_llc qcm_mbm_total qcm_mbm_local dtherm ida arat pln pts hwp_epp pku ospke avx512_vnni md_clear flush_lld arch_capabilities

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
   available: 2 nodes (0-1)
   node 0 cpus: 0 1 2 3 4 5 6 7
   node 0 size: 192120 MB
   node 0 free: 190592 MB
   node 1 cpus: 8 9 10 11 12 13 14 15
   node 1 size: 193508 MB
   node 1 free: 187593 MB
   node distances:
      node   0   1
      0:  10  21
      1:  21  10

(Continued on next page)
### Platform Notes (Continued)

From `/proc/meminfo`

```
MemTotal:       394883680 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
```

From `/etc/*release* /etc/*version*`

```
os-release:
NAME="Red Hat Enterprise Linux"
VERSION="8.1 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.1"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
ANSI_COLOR="0;31"
```

```
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga
```

```
uname -a:
Linux RHEL81-01 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019 x86_64
x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

```
run-level 3 Sep 8 01:51
```

SPEC is set to: `/home/cpu2017`

```
Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda3      xfs   185G   83G  102G  45% /
```

From `/sys/devices/virtual/dmi/id`

```
BIOS: American Megatrends Inc. 3.2 10/18/2019
Vendor: pm_2019-10-08_18:11:34
Product: ppm_2019-10-08_18:11:37
Serial: ps_2019-10-08_18:11:38
```

(Continued on next page)
### Platform Notes (Continued)

Additional information from `dmidecode` follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
- 12x NO DIMM NO DIMM
- 12x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

(End of data from `sysinfo` program)

### Compiler Version Notes

<table>
<thead>
<tr>
<th>Fortran</th>
<th>603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak) 654.roms_s(base, peak)</th>
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### Supermicro

SuperStorage 6029P-E1CR24H
(X11DSC+, Intel Xeon Silver 4215R)

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<td>Supermicro</td>
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<tr>
<td>Hardware Availability</td>
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<td>Software Availability</td>
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### Compiler Version Notes (Continued)

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### Base Compiler Invocation

**C benchmarks:**

`icc`

**Fortran benchmarks:**

`ifort`

**Benchmarks using both Fortran and C:**

`ifort icc`

**Benchmarks using Fortran, C, and C++:**

`icpc icc ifort`

### Base Portability Flags

- `603.bwaves_s: -DSPEC_LP64`
- `607.cactuBSSN_s: -DSPEC_LP64`
- `619.lbm_s: -DSPEC_LP64`
- `621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
- `627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG`
- `628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl`
- `638.imagick_s: -DSPEC_LP64`
- `644.nab_s: -DSPEC_LP64`
- `649.fotonik3d_s: -DSPEC_LP64`
- `654.roms_s: -DSPEC_LP64`
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**Tested by:** Supermicro  
**Test Date:** Sep-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** Apr-2020

### Base Optimization Flags

**C benchmarks:**
- `m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -mbranches-within-32B-boundaries`

**Fortran benchmarks:**
- `m64 -f2l, -z, muldefs -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs -mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

**Benchmarks using both Fortran and C:**

**Benchmarks using Fortran, C, and C++:**

### Peak Compiler Invocation

**C benchmarks:**
- `icc`

**Fortran benchmarks:**
- `ifort`

**Benchmarks using both Fortran and C:**
- `ifort icc`

**Benchmarks using Fortran, C, and C++:**
- `icpc icc ifort`

### Peak Portability Flags

Same as Base Portability Flags
Supermicro
SuperStorage 6029P-E1CR24H
(X11DSC+, Intel Xeon Silver 4215R)

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SPECspeed®2017_fp_peak = 77.3

Peak Optimization Flags

C benchmarks:
619.lbm_s: basepeak = yes
638.imagick_s: basepeak = yes
644.nab_s: -m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -gopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:
603.bwaves_s: -m64 -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -gopenmp -nostandard-realloc-lhs
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
649.fotonik3d_s: Same as 603.bwaves_s
654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:
621.wrf_s: -m64 -std=c11 -Wl,-z,muldefs -prof-gen(pass 1)
-no-prec-div -qopt-prefetch -ipo -xCORE-AVX512 -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
627.cam4_s: basepeak = yes
628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:
607.cactuBSSN_s: basepeak = yes

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Supermicro-Platform-Settings-V1.2-CLX-revG.html
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**Hardware Availability**: Feb-2020  
**Software Availability**: Apr-2020

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