**SPEC CPU®2017 Integer Speed Result**

**Dell Inc.**

PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)

<table>
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<th>SPECspeed®2017_int_peak = 10.3</th>
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<td>perlbench_s</td>
<td>6.38</td>
<td>7.23</td>
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<td>gcc_s</td>
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<td>8.88</td>
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<td>omnetpp_s</td>
<td>13.5</td>
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<td>xalancbmk_s</td>
<td>5.84</td>
<td>13.5</td>
</tr>
<tr>
<td>x264_s</td>
<td>4.89</td>
<td>16.8</td>
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<tr>
<td>deepsjeng_s</td>
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<td>leela_s</td>
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<tr>
<td>exchange2_s</td>
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</tr>
<tr>
<td>xz_s</td>
<td>20.3</td>
<td>20.3</td>
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</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Silver 4215R
- **Max MHz:** 4000
- **Nominal:** 3200
- **Enabled:** 16 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per core
- **Other:** None
- **Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)
- **Storage:** 1 x 1.92 TB SATA SSD
- **Other:** None

**Software**

- **OS:** Red Hat Enterprise Linux 8.1
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++
- **Compiler for Linux:** Fortran: Version 19.1.1.217 of Intel Fortran
- **Parallel:** Yes
- **Firmware:** Version 2.7.7 released May-2020
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** None
- **jemalloc memory allocator V5.0.1**
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage.
# SPEC CPU®2017 Integer Speed Result

Dell Inc.  
PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)  

---

**Spec CPU®2017 Integer Speed Result**  
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## Test Details

<table>
<thead>
<tr>
<th>CPU2017 License</th>
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<tbody>
<tr>
<td>Test Sponsor</td>
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<td>Dell Inc.</td>
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<td>Feb-2020</td>
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## Results Table

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<td><strong>20.3</strong></td>
<td>304</td>
<td>20.3</td>
</tr>
</tbody>
</table>

## Compiler Notes

The inconsistent Compiler Version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOCONF = "retain:true"
OMP_STACKSIZE = "192M"
Dell Inc.  
PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)  

**SPEC CPU®2017 Integer Speed Result**

**SPECspeed®2017_int_base = 10.1**

**SPECspeed®2017_int_peak = 10.3**

---

**General Notes**

Binaries compiled on a system with 1x Intel Core i9–9900K CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5


---

**Platform Notes**

BIOS settings:

- Sub NUMA Cluster enabled
- Virtualization Technology disabled
- System Profile set to Custom
- CPU Performance set to Maximum Performance
- C States set to Autonomous
- C1E disabled
- Uncore Frequency set to Dynamic
- Energy Efficiency Policy set to Performance
- Memory Patrol Scrub disabled
- Logical Processor enabled
- CPU Interconnect Bus Link Power Management disabled
- PCI ASPM L1 Link Power Management disabled
- UPI Prefetch enabled
- LLC Prefetch disabled
- Dead Line LLC Alloc enabled
- Directory AtoS disabled

Sysinfo program `/home/cpu2017/bin/sysinfo`
Rev: r6365 of 2019-08-21 295195f888a3d7edbl6e46a485a0011
running on poweredge-sut-rhel8-1 Fri Jul 17 05:23:13 2020

SUT (System Under Test) info as seen by some common utilities.

For more information on this section, see [https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

---

(Continued on next page)
Dell Inc.

PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

SPECspeed\textsuperscript{®}2017\_int\_base = 10.1
SPECspeed\textsuperscript{®}2017\_int\_peak = 10.3

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Platform Notes (Continued)

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
   2 "physical id"s (chips)
   32 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 16
   physical 0: cores 0 1 2 3 4 5 6 7
   physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture:        x86_64
CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
CPU(s):              32
On-line CPU(s) list: 0-31
Thread(s) per core:  2
Core(s) per socket:  8
Socket(s):           2
NUMA node(s):        2
Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
Stepping:            7
CPU MHz:             2364.862
CPU max MHz:         4000.0000
CPU min MHz:         1000.0000
BogoMIPS:            6400.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            11264K
NUMA node0 CPU(s):   0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30
NUMA node1 CPU(s):   1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl nonstop_tsc cpuid
aem64 pbe xpm

(Continued on next page)
Dell Inc.
PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)

SPEC CPU®2017 Integer Speed Result
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Dell Inc.

PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)

SPECspeed®2017_int_base = 10.1
SPECspeed®2017_int_peak = 10.3

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Platform Notes (Continued)

- cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld

- arch_capabilities

- /proc/cpuinfo cache data
  - cache size : 11264 KB

- From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  - available: 2 nodes (0-1)
  - node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30
  - node 0 size: 192074 MB
  - node 0 free: 190694 MB
  - node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31
  - node 1 size: 193506 MB
  - node 1 free: 191658 MB

- node distances:
  - node   0   1
  - 0:  10  21
  - 1:  21  10

From /proc/meminfo
- MemTotal: 394835400 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
- NAME="Red Hat Enterprise Linux"
- VERSION="8.1 (Ootpa)"
- ID="rhel"
- ID_LIKE="fedora"
- VERSION_ID="8.1"
- PLATFORM_ID="platform:el8"
- PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
- ANSI_COLOR="0;31"

- redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
- system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
- system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

uname -a:
- Linux poweredge-sut-rhel8-1 4.18.0-147.8.1.el8_1.x86_64 #1 SMP Wed Feb 26 03:08:15 UTC 2020 x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

- itlb_multihit: Processor vulnerable
- CVE-2018-3620 (L1 Terminal Fault): Not affected

(Continued on next page)
Dell Inc.

PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
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<td>SPECspeed®2017_int_peak</td>
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</table>

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.
Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Platform Notes (Continued)

Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling
tsx_async_abort: Mitigation: Clear CPU buffers; SMT vulnerable

run-level 3 Jul 16 04:46 last=5

SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
BIOS: Dell Inc. 2.7.7 05/05/2020
Vendor: Dell Inc.
Product: PowerEdge T640
Product Family: PowerEdge
Serial: 1234567

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
14x 002C069D002C 18ASF2G72PDZ-2G9E1 16 GB 2 rank 2933
5x 00AD00B300AD HMA82GR7CJR8N-WM 16 GB 2 rank 2933
1x 00AD063200AD HMA82GR7CJR8N-WM 16 GB 2 rank 2933
4x 00AD069D00AD HMA82GR7CJR8N-WM 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C | 600.perlbench_s(base) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
 | 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Dell Inc.

PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)

| SPECspeed®2017_int_base = 10.1 |
| SPECspeed®2017_int_peak = 10.3 |

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Compiler Version Notes (Continued)

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<tr>
<td>C</td>
<td>600.perlbench_s(peak)</td>
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304
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<table>
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<tr>
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<th>Benchmark(s)</th>
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306
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Base Compiler Invocation

C benchmarks:

icc

(Continued on next page)
Dell Inc.

PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)

**SPEC CPU® 2017 Integer Speed Result**

| SPECspeed®2017_int_base = 10.1 |
| SPECspeed®2017_int_peak = 10.3 |

**CPU2017 License:** 55  
**Test Date:** May-2020  
**Test Sponsor:** Dell Inc.  
**Hardware Availability:** Feb-2020  
**Tested by:** Dell Inc.  
**Software Availability:** Apr-2020

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**Base Compiler Invocation (Continued)**

- **C++ benchmarks:**
  - icpc

- **Fortran benchmarks:**
  - ifort

---

**Base Portability Flags**

- `600.perlbench_s`: -DSPEC_LP64 -DSPEC_LINUX_X64
- `602.gcc_s`: -DSPEC_LP64
- `605.mcf_s`: -DSPEC_LP64
- `620.omnetpp_s`: -DSPEC_LP64
- `623.xalancbmk_s`: -DSPEC_LP64 -DSPEC_LINUX
- `625.x264_s`: -DSPEC_LP64
- `631.deepsjeng_s`: -DSPEC_LP64
- `641.leela_s`: -DSPEC_LP64
- `648.exchange2_s`: -DSPEC_LP64
- `657.xz_s`: -DSPEC_LP64

---

**Base Optimization Flags**

- **C benchmarks:**
  - `-m64 -qnextgen -std=c11`  
  - `-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs`  
  - `-xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops`  
  - `-fuse-ld=gold -qopt-mem-layout-trans=4 -fopenmp -DSPEC_OPENMP`  
  - `-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

- **C++ benchmarks:**
  - `-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries`  
  - `-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse`  
  - `-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4`  
  - `-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin`  
  - `-lqkmalloc`

- **Fortran benchmarks:**
  - `-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -xCORE-AVX512`  
  - `-O3 -ipo -no-prec-div -qopt-mem-layout-trans=4`  
  - `-nostandard-realloc-lhs -align array32byte`  
  - `-mbranches-within-32B-boundaries`
Dell Inc.

PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)

SPEC CPU®2017 Integer Speed Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECspeed®2017_int_base = 10.1
SPECspeed®2017_int_peak = 10.3

CPU2017 License: 55
Test Sponsor: Dell Inc.
Test Date: May-2020
Tested by: Dell Inc.
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64(*) -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

(*) Indicates a portability flag that was found in a non-portability variable.

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
-xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-strict-overflow
-mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

602.gcc_s: -m64 -qnextgen -std=c11 -fuse-ld=gold
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fprofile-generate(pass 1)
-fprofile-use=default.profdata(pass 2) -xCORE-AVX512 -flto
-Ofast(pass 1) -O3 -ffast-math -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

(Continued on next page)
Dell Inc.

PowerEdge T640 (Intel Xeon Silver 4215R, 3.20 GHz)

| SPECspeed\textsuperscript{\textregistered}2017_int_base | 10.1 |
| SPECspeed\textsuperscript{\textregistered}2017_int_peak | 10.3 |

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Peak Optimization Flags (Continued)

605.mcf\_s: basepeak = yes

625.x264\_s: -m64 -qnextgen -std=c11
-Wl, -plugin-opt=-x86-branches-within-32B-boundaries
-Wl, -z, muldefs -xCORE-AVX512 -flto -O3 -ffast-math
-fuse-ld=gold -qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

657.xz\_s: basepeak = yes

C++ benchmarks:

620.omnetpp\_s: basepeak = yes

623.xalancbmk\_s: basepeak = yes

631.deepsjeng\_s: basepeak = yes

641.leela\_s: basepeak = yes

Fortran benchmarks:

648.exchange2\_s: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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