**SPEC CPU®2017 Integer Rate Result**

**Dell Inc.**

PowerEdge R440 (Intel Xeon Bronze 3204, 1.90 GHz)

**SPECrater®2017_int_base = 44.2**

**SPECrater®2017_int_peak = 45.2**

---

**CPU2017 License:**  55

**Test Sponsor:**  Dell Inc.

**Tested by:**  Dell Inc.

**Test Date:**  Jul-2020

**Hardware Availability:**  Jul-2020

**Software Availability:**  Apr-2020

### Copies

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<td>557.xz_r</td>
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</tbody>
</table>

---

**Hardware**

- **CPU Name:** Intel Xeon Bronze 3204
- **Max MHz:** 1900
- **Nominal:** 1900
- **Enabled:** 12 cores, 2 chips
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 8.25 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-3200AA-R, running at 2133)
- **Storage:** 1 x 1.92 TB SATA SSD
- **Other:** None

**Software**

- **OS:** Red Hat Enterprise Linux 8.1
- **kernel 4.18.0-147.el8.x86_64**
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 2.7.7 released May-2020
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** None
- **jemalloc memory allocator V5.0.1**
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage.
Dell Inc.

PowerEdge R440 (Intel Xeon Bronze 3204, 1.90 GHz)

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

SPECrate®2017_int_base = 44.2
SPECrate®2017_int_peak = 45.2

Test Date: Jul-2020
Hardware Availability: Jul-2020
Software Availability: Apr-2020

### Results Table

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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.

The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.

For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

MALLOC_CONF = "retain:true"
```
General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache syncd and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
  numactl --interleave=all runcpu <etc>
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS settings:
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub set to standard
CPU Interconnect Bus Link Power Management disabled
PCI ASPM L1 Link Power Management disabled
UPI Prefetch enabled
LLC Prefetch disabled
Dead Line LLC Alloc enabled
Directory AtoS disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edba6e46a485a0011
running on localhost.localdomain Mon Jul 13 09:48:33 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
  https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Bronze 3204 CPU @ 1.90GHz

(Continued on next page)
Dell Inc.

PowerEdge R440 (Intel Xeon Bronze 3204, 1.90 GHz)

SPEC®CPU2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Dell Inc.

PowerEdge R440 (Intel Xeon Bronze 3204, 1.90 GHz)

SPECrate®2017_int_base = 44.2
SPECrate®2017_int_peak = 45.2

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Jul-2020
Hardware Availability: Jul-2020
Software Availability: Apr-2020

Platform Notes (Continued)

2 "physical id"s (chips)
12 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 6
siblings : 6
physical 0: cores 0 1 2 3 4 5
physical 1: cores 0 1 2 3 4 5

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 12
On-line CPU(s) list: 0-11
Thread(s) per core: 1
Core(s) per socket: 6
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Bronze 3204 CPU @ 1.90GHz
Stepping: 7
CPU MHz: 1871.139
CPU max MHz: 1900.0000
CPU min MHz: 800.0000
BogoMIPS: 3800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 8448K
NUMA node0 CPU(s): 0,2,4,6,8,10
NUMA node1 CPU(s): 1,3,5,7,9,11
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

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Platform Notes (Continued)

/proc/cpuinfo cache data
  cache size : 8448 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 2 4 6 8 10
  node 0 size: 192076 MB
  node 0 free: 191322 MB
  node 1 cpus: 1 3 5 7 9 11
  node 1 size: 193508 MB
  node 1 free: 192603 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 394839092 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux"
    VERSION="8.1 (Ootpa)"
    ID="rhel"
    ID_LIKE="fedora"
    VERSION_ID="8.1"
    PLATFORM_ID="platform:el8"
    PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
    ANSI_COLOR="0;31"
  redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
  system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

uname -a:
  Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled

(Continued on next page)
SPEC CPU®2017 Integer Rate Result

Dell Inc.

PowerEdge R440 (Intel Xeon Bronze 3204, 1.90 GHz)  
SPECraté®2017_int_base = 44.2  
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CPU2017 License: 55  
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Software Availability: Apr-2020

Platform Notes (Continued)

CVE-2017-5753 (Spectre variant 1):  
mitigation: usercopy/swapgs barriers and __user pointer sanitation

CVE-2017-5715 (Spectre variant 2):  
mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Jul 13 04:36 last=5

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 1.7T 23G 1.7T 2% /home

From /sys/devices/virtual/dmi/id
BIOS: Dell Inc. 2.7.7 05/06/2020
Vendor: Dell Inc.
Product: PowerEdge R440
Product Family: PowerEdge
Serial: F9TD613

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
12x 002C069D002C 36ASF4G72PZ-3G2E2 32 GB 2 rank 3200
4x Not Specified Not Specified

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base)
------------------------------------------------------------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

(Continued on next page)
Dell Inc.

PowerEdge R440 (Intel Xeon Bronze 3204, 1.90 GHz)

Compiler Version Notes (Continued)

------------------------------------------------------------------------------
C | 500.perlbench_r(peak) 557.xz_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
C | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen
Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
    | 525.x264_r(base, peak) 557.xz_r(base)
------------------------------------------------------------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
C | 500.perlbench_r(peak) 557.xz_r(peak)
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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C | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base, peak)
    | 525.x264_r(base, peak) 557.xz_r(base)
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Dell Inc.

PowerEdge R440 (Intel Xeon Bronze 3204, 1.90 GHz)

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CPU2017 License: 55
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Compiler Version Notes (Continued)

Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
C       | 500.perlbench_r(peak) 557.xz_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak)
        | 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort
## SPEC CPU®2017 Integer Rate Result

**Dell Inc.**  
PowerEdge R440 (Intel Xeon Bronze 3204, 1.90 GHz)  

**SPECrate®2017_int_base = 44.2**  
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</table>

### Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64  
548.exchange2_r: -DSPEC_LP64  
557.xz_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

- m64 -gnextgen -std=c11  
- Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs  
- xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops  
- fuse-ld=gold -qopt-mem-layout-trans=4  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin  
- lqkmalloc

**C++ benchmarks:**

- m64 -gnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries  
- Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse  
- funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin  
- lqkmalloc

**Fortran benchmarks:**

- m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs  
- xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4  
- nostandard-realloc-lhs -align array32byte -auto  
- mbranches-within-32B-boundaries  
- L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin  
- lqkmalloc

### Peak Compiler Invocation

**C benchmarks:**

icc

*(Continued on next page)*
Peak Compiler Invocation (Continued)

C++ benchmarks:
  icpc

Fortran benchmarks:
  ifort

Peak Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -D_FILE_OFFSET_BITS=64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

500.perlbench_r: -W1,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2)
  -xCORE-AVX512 -ipo -O3 -no-prec-div
  -qopt-mem-layout-trans=4 -fno-strict-overflow
  -mbranches-within-32B-boundaries
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
  -lqkmalloc

502.gcc_r: -m32
  -L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/ia32_lin
  -std=gnu89
  -W1, -plugin-opt=-x86-branches-within-32B-boundaries
  -W1,-z,muldefs -fprofile-generate(pass 1)
  -fprofile-use=default.profdatalinux2 -xCORE-AVX512 -flto
  -Ofast(pass 1) -O3 -ffast-math -qnextgen -fuse-ld=gold
  -qopt-mem-layout-trans=4 -L/usr/local/jemalloc32-5.0.1/lib
  -ljemalloc

505.mcf_r: basepeak = yes

(Continued on next page)
Dell Inc.

PowerEdge R440 (Intel Xeon Bronze 3204, 1.90 GHz)

| SPECrate®2017_int_base = 44.2 |
| SPECrate®2017_int_peak = 45.2 |

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.
Test Date: Jul-2020
Hardware Availability: Jul-2020
Software Availability: Apr-2020

Peak Optimization Flags (Continued)

525.x264_r: -m64 -qnextgen -std=c11
- W1,-plugin-opt=-x86-branches-within-32B-boundaries
- W1,-z,muldefs -xCORE-AVX512 -flto -O3 -ffast-math
- fuse-ld=gold -qopt-mem-layout-trans=4 -fno-alias
- L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
  -lqkmalloc

557.xz_r: -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
- qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
- L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
  -lqkmalloc

C++ benchmarks:

520.omnetpp_r: basepeak = yes
523.xalancbmk_r: basepeak = yes
531.deepsjeng_r: basepeak = yes
541.leela_r: basepeak = yes

Fortran benchmarks:

548.exchange2_r: basepeak = yes

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.