# SPEC CPU® 2017 Floating Point Speed Result

## Dell Inc.

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

<table>
<thead>
<tr>
<th>threads</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>32</td>
<td>130</td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>32</td>
<td>80.3</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>32</td>
<td>104</td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>32</td>
<td>115</td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>32</td>
<td>70.9</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>32</td>
<td>63.5</td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>32</td>
<td>88.7</td>
</tr>
<tr>
<td>644.nab_s</td>
<td>32</td>
<td>167</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>32</td>
<td>73.9</td>
</tr>
<tr>
<td>654.roms_s</td>
<td>32</td>
<td>128</td>
</tr>
</tbody>
</table>

## Hardware

- **CPU Name:** Intel Xeon Silver 4216
- **Max MHz:** 3200
- **Nominal:** 2100
- **Enabled:** 32 cores, 2 chips
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Memory:** 384 GB (12 x 32 GB 2Rx8 PC4-3200V-R, running at 2400)
- **Storage:** 1 x 1.92 TB SATA SSD
- **Other:** None

## Software

- **OS:** Red Hat Enterprise Linux 8.1
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 2.7.7 released May-2020
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
Dell Inc.

PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECspeed®2017_fp_base = 111
SPECspeed®2017_fp_peak = 112

Results Table

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Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
MALLOC_CONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-9900K CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
Dell Inc.  
PowerEdge R440 (Intel Xeon Silver 4216, 2.10 GHz)  

**SPEC CPU®2017 Floating Point Speed Result**

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<thead>
<tr>
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<th>SPECspeed®2017_fp_peak</th>
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<td>111</td>
<td>112</td>
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**CPU2017 License:** 55

**Test Sponsor:** Dell Inc.

**Test Date:** Apr-2020

**Tested by:** Dell Inc.

**Hardware Availability:** Apr-2020

**Software Availability:** Apr-2020

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**General Notes (Continued)**

- is mitigated in the system as tested and documented.
- Transparent Huge Pages enabled by default
- Prior to runcpu invocation
- Filesystem page cache synced and cleared with:
  ```
  sync; echo 3> /proc/sys/vm/drop_caches
  ```
- runcpu command invoked through numactl i.e.:
  ```
  numactl --interleave=all runcpu <etc>
  ```
- jemalloc, a general purpose malloc implementation
- built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

---

**Platform Notes**

- BIOS settings:
- Virtualization Technology disabled
- System Profile set to Custom
- CPU Performance set to Maximum Performance
- C States set to Autonomous
- C1E disabled
- Uncore Frequency set to Dynamic
- Energy Efficiency Policy set to Performance
- Memory Patrol Scrub set to standard
- Logical Processor disabled
- CPU Interconnect Bus Link Power Management disabled
- PCI ASPM L1 Link Power Management disabled
- UPI Prefetch enabled
- LLC Prefetch disabled
- Dead Line LLC Alloc enabled
- Directory AtoS disabled

- Sysinfo program /home/cpu2017/bin/sysinfo
- Rev: r6365 of 2019-08-21 295195f888a3d7edbl6e46a485a0011
- running on localhost.localdomain Sun Jun 14 21:20:56 2020

- SUT (System Under Test) info as seen by some common utilities.
  - For more information on this section, see
  - https://www.spec.org/cpu2017/Docs/config.html#sysinfo

- From /proc/cpuinfo
  ```
  model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2 *physical id"s (chips)
  32 *processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 16
  siblings : 16
  ```

(Continued on next page)
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Platform Notes (Continued)

physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 1
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2891.618
CPU max MHz: 3200.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30
NUMA node1 CPU(s): 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lg12 tsc_lcm xtpr pdcm dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
inle vpclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_pit intelmpi ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnni
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cmmpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl vsxveopt xsaveopt xsaveopt xsaves qemuc lcs qemuc_occmap lcs
qemuc_mbmaximal qemuc_msm_local dtimer ida arat lld arat pts pkau ospe avx512_vnni
md_clear flush_lld
arch_capabilities

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

(Continued on next page)
Dell Inc.

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Platform Notes (Continued)

available: 2 nodes (0-1)
node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30
node 0 size: 192074 MB
node 0 free: 184422 MB
node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31
node 1 size: 193506 MB
node 1 free: 192528 MB
node distances:
  node 0 1
  0: 10 21
  1: 21 10

From /proc/meminfo
MemTotal: 394835328 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

OS-Release:
NAME="Red Hat Enterprise Linux"
VERSION="8.1 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.1"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
ANSI_COLOR="0;31"

redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

uname -a:
Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

(Continued on next page)
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Platform Notes (Continued)

run-level 3 Jun 14 16:22 last=5

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 1.7T 29G 1.7T 2% /home

From /sys/devices/virtual/dmi/id
BIOS: Dell Inc. 2.7.7 05/06/2020
Vendor: Dell Inc.
Product: PowerEdge R440
Product Family: PowerEdge
Serial: F9TD613

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
12x 002C069D002C 36ASF4G72PZ-3G2E2 32 GB 2 rank 3200
4x Not Specified Not Specified

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
               | 644.nab_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------

C++, C, Fortran | 607.cactuBSSN_s(base, peak)
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

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| SPEC CPU®2017 fp_base = 111 |
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CPU2017 License: 55
Test Sponsor: Dell Inc.
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---

Base Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

---

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian

(Continued on next page)
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Copyright 2017-2020 Standard Performance Evaluation Corporation

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Base Portability Flags (Continued)

627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries

Fortran benchmarks:
-m64 -Wl,-z,muldefs -DSPEC_OPENMP -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both Fortran and C:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
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Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -Wl,-z,muldefs -xCORE-AVX2 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc

Fortran benchmarks:
ifort

(Continued on next page)
Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

619.lbm_s: basepeak = yes

638.imagick_s: basepeak = yes

644.nab_s: -m64 -std=c11 -Wl,-z,muldeps -xCORE-AVX2 -ipo -O3
-no-pref-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -openmp -DSPEC_OPENMP
-mbraches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:

603.bwaves_s: -m64 -Wl,-z,muldeps -prof-gen(pass 1) -prof-use(pass 2)
-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -ipo -xCORE-AVX2
-03 -no-pref-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -openmp -nostandard-realloc-lhs
-mbraches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: basepeak = yes

Benchmarks using both Fortran and C:

621.wrf_s: -m64 -std=c11 -Wl,-z,muldeps -prof-gen(pass 1)
 prof-use(pass 2) -ipo -xCORE-AVX2 -03 -no-pref-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
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**Software Availability:** Apr-2020

## Peak Optimization Flags (Continued)

621.wrf_s (continued):
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-mbranches-within-32B-boundaries -nostandard-realloc-lhs
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

627.cam4_s: basepeak = yes

628.pop2_s: basepeak = yes

Benchmarks using Fortran, C, and C++:

607.cactuBSSN_s: basepeak = yes

---

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml  

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-06-14 22:20:55-0400.  
Originally published on 2020-07-07.