**SPEC CPU®2017 Integer Speed Result**

**Lenovo Global Technology**

**ThinkSystem ST550**  
(2.40 GHz, Intel Xeon Silver 4210R)

**SPECspeed®2017_int_base** = **8.82**  
**SPECspeed®2017_int_peak** = **Not Run**

---

**Test Sponsor:** Lenovo Global Technology  
**Tested by:** Lenovo Global Technology

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_int_base (8.82)</th>
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<td>7.00</td>
<td>13.5</td>
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<tr>
<td>8.00</td>
<td>18.6</td>
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</table>

---

**Hardware**

**CPU Name:** Intel Xeon Silver 4210R  
**Max MHz:** 3200  
**Nominal:** 2400  
**Enabled:** 20 cores, 2 chips, 2 threads/core  
**Orderable:** 1.2 chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**Cache L2:** 1 MB I+D on chip per core  
**Cache L3:** 13.75 MB I+D on chip per chip  
**Other:** None  
**Memory:** 192 GB (12 x 16 GB 2Rx8 PC4-2933Y-R, running at 2400)  
**Storage:** 1 x 480 GB SATA SSD  
**Other:** None

---

**Software**

**OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)  
**Kernel:** 4.12.14-195-default  
**Compiler:**  
C/C++: Version 19.1.1.217 of Intel C/C++  
Fortran: Version 19.1.1.217 of Intel Fortran

**Compiler for Linux:**  
Yes

**Parallel:** Yes

**Firmware:** Lenovo BIOS Version 00E155L 2.61 released May-2020

**File System:** xfs

**System State:** Run level 3 (multi-user)

**Base Pointers:** 64-bit

**Peak Pointers:** Not Applicable

**Other:** jemalloc memory allocator V5.0.1

**Power Management:** BIOS set to prefer performance at the cost of additional power usage
Lenovo Global Technology
ThinkSystem ST550
(2.40 GHz, Intel Xeon Silver 4210R)

SPECspeed®2017_int_base = 8.82
SPECspeed®2017_int_peak = Not Run

Results Table

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</table>

SPECspeed®2017_int_base = 8.82
SPECspeed®2017_int_peak = Not Run

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017-1.1.0-ic19.1.1/lib/intel64:/home/cpu2017-1.1.0-ic19.1.1/j
e5.0.1-64"
MALLOCONF = "retain:true"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0 Transparent Huge Pages enabled by default Prior to runcpu invocation Filesystem page cache synced and cleared with:
Lenovo Global Technology
ThinkSystem ST550
(2.40 GHz, Intel Xeon Silver 4210R)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

General Notes (Continued)

sync; echo 3>>/proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3640 (Spectre variant 3a) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3639 (Spectre variant 4) is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation

Platform Notes

BIOS configuration:
Choose Operating Mode set to Maximum Performance and then set it to Custom Mode
Stale AtoS set to Enable
LLC dead line alloc set to Disable
Patrol Scrub set to Disable
C-States set to Legacy

Sysinfo program /home/cpu2017-1.1.0-ic19.1.1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1b6e6a485a0011
running on linux-9n08 Mon Jun 1 14:17:30 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see 
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
 2 *physical id"s (chips)
 40 *processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit

(Continued on next page)
## Platform Notes (Continued)

- **Byte Order:** Little Endian
- **Address sizes:** 46 bits physical, 48 bits virtual
- **CPU(s):** 40
- **On-line CPU(s) list:** 0-39
- **Thread(s) per core:** 2
- **Core(s) per socket:** 10
- **Socket(s):** 2
- **NUMA node(s):** 2
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
- **Stepping:** 7
- **CPU MHz:** 2400.000
- **CPU max MHz:** 3200.0000
- **CPU min MHz:** 1000.0000
- **BogoMIPS:** 4800.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 14080K
- **NUMA node0 CPU(s):** 0-9,20-29
- **NUMA node1 CPU(s):** 10-19,30-39
- **Flags:**
  - fpu
  - vme
  - de
  - pse
  - tsc
  - msr
  - pae
  - mce
  - cx8
  - apic
  - sep
  - mtrr
  - pge
  - mca
  - cmov
  - pat
  - pse36
  - clflush
  - dts
  - acpi
  - mmx
  - fxsr
  - sse
  - sse2
  - ss
  - ht
  - tm
  - pbe
  - syscall
  - nx
  - pdpe1gb
  - rdtscp
  - adx
  - lm
  - constant_tsc
  - arch
  - perf
  - fru
  - srbape
  - stribp
  - stibp
  - ept
  - smep
  - bmi2
  - msa
  - resv
  - aperfmperf
  - pkclmulqdq
  - dates64
  - monitor
  - ds CPL
  - vmx
  - smx
  - est
  - tm2
  - ssse3
  - sdbg
  - fma
  - cx16
  - xtpr
  - pdcm
  - pcid
  - dca
  - sse4_1
  - sse4_2
  - x2apic
  - movbe
  - popcnt
  - tsc_deadline_timer
  - aes
  - xsave
  - avx
  - f16c
  - rdrand
  - lahf_lm
  - abm
  - 3nowprefetch
  - cpuid_fault
  - epb
  - cat_13
  - cdp_13
  - invvpctid
  - single
  - intel_ppin
  - ssbd
  - mba
  - ibpb
  - stibp
  - ibrs
  - enhanced
  - tpr
  - shadow
  - vmni
  - flexpriority
  - ept
  - vpid
  - fsgsbase
  - tsc_adjust
  - bmi1
  - hle
  - avx2
  - smep
  - bmi2
  - erms
  - invpcid
  - rtm
  - cmp
  - mpx
  - rdt_a
  - avx512f
  - avx512dq
  - rdseed
  - adx
  - smap
  - clflushopt
  - clwb
  - intel_pt
  - avx512cd
  - avx512bw
  - avx512vl
  - xsaveopt
  - xsavec
  - xgetbv1
  - xsave
  - cmq
  - llc
  - cmp
  - occcup
  - llc
  - cmq
  - mbm
  - total
  - cmq
  - mbm
  - local
  - dtherm
  - ida
  - arat
  - pln
  - pts
  - pku
  - ospke
  - avx512
  - vnni
  - md
  - clear
  - flush
  - lld
  - arch
  - capabilities

/proc/cpuinfo cache data
- **cache size:** 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
- **available:** 2 nodes (0-1)
- **node 0 cpus:** 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
- **node 0 size:** 96384 MB
- **node 0 free:** 95754 MB
- **node 1 cpus:** 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39

(Continued on next page)
Lenovo Global Technology
ThinkSystem ST550
(2.40 GHz, Intel Xeon Silver 4210R)

SPECspeed®2017_int_base = 8.82
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Test by: Lenovo Global Technology

Platform Notes (Continued)

node 1 size: 96733 MB
node 1 free: 96467 MB
node distances:
node 0 1
0: 10 21
1: 21 10

From /proc/meminfo
MemTotal: 197753124 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux linux-9n08 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Jun 1 14:16

SPEC is set to: /home/cpu2017-1.1.0-ic19.1.1

From /sys/devices/virtual/dmi/id
BIOS: Lenovo -[00E155L-2.61]- 05/20/2020
Vendor: Lenovo

(Continued on next page)
Lenovo Global Technology
ThinkSystem ST550 (2.40 GHz, Intel Xeon Silver 4210R)

SPECSpeed®2017_int_base = 8.82
SPECSpeed®2017_int_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Test Date: Jun-2020
Hardware Availability: Mar-2020
Software Availability: Apr-2020

Platform Notes (Continued)

Product: ThinkSystem ST550 -[7X09TOZ000]-
Product Family: ThinkSystem
Serial: 1234567890

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
12x SK Hynix HMA82GR7CJR8N-WM 16 GB 2 rank 2933

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
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<tr>
<th>C</th>
<th>600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base) 657.xz_s(base)</th>
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<tbody>
<tr>
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<tr>
<td>Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1</td>
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<tr>
<td>NextGen Build 20200304</td>
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<tr>
<td>Copyright (C) 1985-2020 Intel Corporation. All rights reserved.</td>
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|==============================================================================
| C++     | 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base) 641.leela_s(base)        |
|         |                                                                                             |
| Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1              |
| NextGen Build 20200304                                                                    |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.                            |
|                                                                                             |
|==============================================================================
| Fortran | 648.exchange2_s(base)                                                                     |
|         |                                                                                             |
| Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.1.1.217 Build 20200306 |
| Copyright (C) 1985-2020 Intel Corporation. All rights reserved.                            |

Base Compiler Invocation

C benchmarks:
icc

(Continued on next page)
Base Compiler Invocation (Continued)

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -ftlo -mfpmath=sse -funroll-loops
-fuse-ld=gold -qopt-mem-layout-trans=4 -fopenmp -DSPEC_OPENMP
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -ftlo -mfpmath=sse
-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -xCORE-AVX512
-O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte
-mbranches-within-32B-boundaries
# Lenovo Global Technology

## ThinkSystem ST550 (2.40 GHz, Intel Xeon Silver 4210R)

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**CPU2017 License:** 9017  
**Test Sponsor:** Lenovo Global Technology  
**Tested by:** Lenovo Global Technology

| Test Date: | Jun-2020 |
| Test Sponsor: | Lenovo Global Technology |
| Hardware Availability: | Mar-2020 |
| Software Availability: | Apr-2020 |

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:
- [http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-H.xml](http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-H.xml)

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-06-01 02:17:29-0400.
Originally published on 2020-06-23.