# SPEC CPU®2017 Floating Point Rate Result

**Dell Inc.**

PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz)

| CPU2017 License: | 55 |
| Test Sponsor: | Dell Inc. |
| Tested by: | Dell Inc. |
| Test Date: | May-2020 |
| Hardware Availability: | Feb-2020 |
| Software Availability: | Apr-2020 |

<table>
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<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<tr>
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<td>507.cactuBSSN_r</td>
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## Hardware

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<th>Description</th>
<th>Value</th>
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<tr>
<td>CPU Name</td>
<td>Intel Xeon Gold 6246R</td>
</tr>
<tr>
<td>Max MHz</td>
<td>4100</td>
</tr>
<tr>
<td>Nominal</td>
<td>3400</td>
</tr>
<tr>
<td>Enabled</td>
<td>32 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable</td>
<td>1,2 chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3</td>
<td>35.75 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>768 GB (24 x 32 GB 2Rx8 PC4-2933V-R, running at 2933)</td>
</tr>
<tr>
<td>Storage</td>
<td>1 x 960 GB SATA SSD</td>
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<tr>
<td>Other</td>
<td>None</td>
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## Software

<table>
<thead>
<tr>
<th>Description</th>
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<tr>
<td>OS</td>
<td>Red Hat Enterprise Linux 8.1</td>
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<tr>
<td>Compiler</td>
<td>C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel</td>
<td>No</td>
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<tr>
<td>Firmware</td>
<td>Version 2.7.1 released Feb-2020</td>
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<tr>
<td>File System</td>
<td>tmpfs</td>
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<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
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<tr>
<td>Base Pointers</td>
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<tr>
<td>Peak Pointers</td>
<td>64-bit</td>
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<tr>
<td>Other</td>
<td>jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Power Management</td>
<td>BIOS set to prefer performance at the cost of additional power usage</td>
</tr>
</tbody>
</table>
**SPEC CPU®2017 Floating Point Rate Result**

**Dell Inc.**

PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz)

**Results Table**

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<th>Benchmark</th>
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</table>

**Compiler Notes**

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = 
"/dev/shm/cpu2017-ic19.1u1/lib/intel64:/dev/shm/cpu2017-ic19.1u1/je5.0.1-64"

MALLOC_CONF = "retain:true"
```
General Notes

Binaries compiled on a system with 1x Intel Core i9-9900K CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
  numactl --interleave=all runcpu <etc>
Benchmark run from a 225 GB ramdisk created with the cmd; "mount -t tmpfs -o size=225G tmpfs /mnt/ramdisk"
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS settings:
Sub NUMA Cluster enabled
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub set to standard
Logical Processor enabled
CPU Interconnect Bus Link Power Management disabled
PCI ASPM L1 Link Power Management disabled
UPI Prefetch enabled
LLC Prefetch disabled
Dead Line LLC Alloc enabled
Directory AtoS disabled

Sysinfo program /dev/shm/cpu2017-ic19.1u1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbb1e6e46a485a0011
running on localhost.localdomain Tue May 26 18:00:32 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
  https://www.spec.org/cpu2017/Docs/config.html#sysinfo

(Continued on next page)
Dell Inc.

PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz)

Dell Inc.  SPECrate®2017_fp_base = 245

SPECrate®2017_fp_peak = 256

CPU2017 License: 55  Test Date: May-2020
Test Sponsor: Dell Inc.  Hardware Availability: Feb-2020
Tested by: Dell Inc.  Software Availability: Apr-2020

Platform Notes (Continued)

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz
2 "physical id"s (chips)
64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 6 12 13 16 17 18 19 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 13 16 17 18 19 21 24 28 29

From lscpu:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6246R CPU @ 3.40GHz
Stepping: 7
CPU MHz: 3813.552
CPU max MHz: 4100.0000
CPU min MHz: 1200.0000
BogoMIPS: 6800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0,4,6,12,16,20,24,28,32,36,38,44,48,52,56,60
NUMA node1 CPU(s): 1,5,9,13,17,21,25,29,33,37,41,45,49,53,57,61
NUMA node2 CPU(s): 2,8,10,14,18,22,26,30,34,40,42,46,50,54,58,62
NUMA node3 CPU(s): 3,7,11,15,19,23,27,31,35,39,43,47,51,55,59,63
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp cpe

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SPEC CPU®2017 Floating Point Rate Result

Dell Inc.
PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz)

Copyright 2017-2020 Standard Performance Evaluation Corporation

Dell Inc.

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

SPECrate®2017_fp_base = 245
SPECrate®2017_fp_peak = 256

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Platform Notes (Continued)

flexpriority ept vpid fsbgbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cq n px rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsaves cqm_llc cqm_occu llc cqm_mb m_total

cqm mb m_local dtherm ida pln pts pku ospke avx512_vnni md_clear flush lld
arch_capabilities

/cache/data

cache size: 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 4 6 12 16 20 24 28 32 36 38 44 48 52 56 60
node 0 size: 192046 MB
node 0 free: 191038 MB
node 1 cpus: 1 5 9 13 17 21 25 29 33 37 41 45 49 53 57 61
node 1 size: 193532 MB
node 1 free: 182595 MB
node 2 cpus: 2 8 10 14 18 22 26 30 34 40 42 46 50 54 58 62
node 2 size: 193532 MB
node 2 free: 192734 MB
node 3 cpus: 3 7 11 15 19 23 27 31 35 39 43 47 51 55 59 63
node 3 size: 193532 MB
node 3 free: 193289 MB
node distances:
node 0 1 2 3
0: 10 21 11 21
1: 21 10 21 11
2: 11 21 10 21
3: 21 11 21 10

From /proc/meminfo

MemTotal: 791187572 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

os-release:
NAME="Red Hat Enterprise Linux"
VERSION="8.1 (Ootpa)"
ID="rhel"
ID_LIKE="fedora"
VERSION_ID="8.1"
PLATFORM_ID="platform:el8"
PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)

(Continued on next page)
Dell Inc.

PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz)

SPEC CPU®2017 Floating Point Rate Result

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Dell Inc.

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

SPECrate®2017_fp_base = 245
SPECrate®2017_fp_peak = 256

Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Platform Notes (Continued)

system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

uname -a:
Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user pointer sanitation
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 May 26 13:27

SPEC is set to: /dev/shm/cpu2017-ic19.1u1

Filesystem Type Size Used Avail Use% Mounted on
tmpfs tmpfs 378G 4.2G 374G 2% /dev/shm

From /sys/devices/virtual/dmi/id
BIOS: Dell Inc. 2.7.1 02/14/2020
Vendor: Dell Inc.
Product: PowerEdge MX740c
Product Family: PowerEdge
Serial: 1234567

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
21x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
1x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
2x 00AD069D00AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933

(End of data from sysinfo program)
Dell Inc.
PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz)

SPECrate®2017_fp_base = 245
SPECrate®2017_fp_peak = 256

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.
Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
 | 544.nab_r(base, peak)
==============================================================================
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C          | 511.povray_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
NextGen Build 20200304

(Continued on next page)
Compiler Version Notes (Continued)

Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

==============================================================================
C++, C          | 511.povray_r(peak)
-----------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
    Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
    Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
    NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
    NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
    64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base, peak)
==============================================================================
Fortran Intel(R) 64 Compiler for applications running on Intel(R)
    64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
    64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
    NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
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### Dell Inc.

**PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz)**

<table>
<thead>
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#### SPEC CPU®2017 Floating Point Rate Result

**SPECrate®2017_fp_base = 245**

**SPECrate®2017_fp_peak = 256**

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### Compiler Version Notes (Continued)

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### Base Compiler Invocation

**C benchmarks:**
- icc

**C++ benchmarks:**
- icpc

**Fortran benchmarks:**
- ifort

(Continued on next page)
## Dell Inc. PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz)

### SpecCpu 2017 Floating Point Rate Result

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**Test Date:** May-2020  
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### Base Compiler Invocation (Continued)

Benchmarks using both Fortran and C:

```
ifort icc
```

Benchmarks using both C and C++:

```
icpc icc
```

Benchmarks using Fortran, C, and C++:

```
icpc icc ifort
```

### Base Portability Flags

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

```
-m64 -m64 -mnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

**C++ benchmarks:**

```
-m64 -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
```

**Fortran benchmarks:**

```
-m64 -flto
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
```

(Continued on next page)
## Base Optimization Flags (Continued)

- Fortran benchmarks (continued):
  ```
  -fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
  -qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
  -auto -mbranches-within-32B-boundaries
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
  ```

- Benchmarks using both Fortran and C:
  ```
  -m64 -qnxtgen -std=c11
  -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
  -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
  -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
  -qopt-prefetch -ffinite-math-only
  -qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
  -align array32byte -auto -mbranches-within-32B-boundaries
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
  ```

- Benchmarks using both C and C++:
  ```
  -m64 -qnxtgen -std=c11
  -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
  -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
  -funroll-loops -qopt-mem-layout-trans=4
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
  ```

- Benchmarks using Fortran, C, and C++:
  ```
  -m64 -qnxtgen -std=c11
  -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
  -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
  -funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
  -qopt-prefetch -ffinite-math-only
  -qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
  -align array32byte -auto -mbranches-within-32B-boundaries
  -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc
  ```

### Peak Compiler Invocation

- C benchmarks:
  ```
  icc
  ```

- C++ benchmarks:
  ```
  icpc
  ```

- Fortran benchmarks:
  ```
  ifort
  ```

(Continued on next page)
Dell Inc. 
PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz) 

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**Peak Compiler Invocation (Continued)**

Benchmarks using both Fortran and C: 
ifort icc

Benchmarks using both C and C++: 
icpc icc

Benchmarks using Fortran, C, and C++: 
icpc icc ifort

**Peak Portability Flags**

Same as Base Portability Flags

**Peak Optimization Flags**

C benchmarks:

- 519.lbm_r: basepeak = yes
- 538.imagick_r: basepeak = yes
- 544.nab_r: basepeak = yes

C++ benchmarks:

- 508.namd_r: basepeak = yes

- 510.parest_r: -m64 -qnextgen
- -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
- -Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast
- -ffast-math -fto -mfpmath=sse -funroll-loops
- -qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/lib
- -ljemalloc

Fortran benchmarks:

- 303.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
- -Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo
- -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles

(Continued on next page)
**Dell Inc.**

PowerEdge MX740C (Intel Xeon Gold 6246R, 3.40 GHz)

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**Test Sponsor:** Dell Inc.

**Tested by:** Dell Inc.

**Test Date:** May-2020

**Hardware Availability:** Feb-2020

**Software Availability:** Apr-2020

### Peak Optimization Flags (Continued)

503.bwaves_r (continued):
- -qopt-mem-layout-trans=4 -nostandard-realloc-lhs
- -align array32byte -auto -mbranches-within-32B-boundaries
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

**Benchmarks using both Fortran and C:**

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
- -ipo -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles
- -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
- -nostandard-realloc-lhs -align array32byte -auto
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

527.cam4_r: basepeak = yes

**Benchmarks using both C and C++:**

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
- -ipo -no-prec-div -qopt-prefetch -ffinite-math-only
- -qopt-multiple-gather-scatter-by-shuffles
- -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
- -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

526.blender_r: basepeak = yes

**Benchmarks using Fortran, C, and C++:**

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at


You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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