SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

Dell Inc.

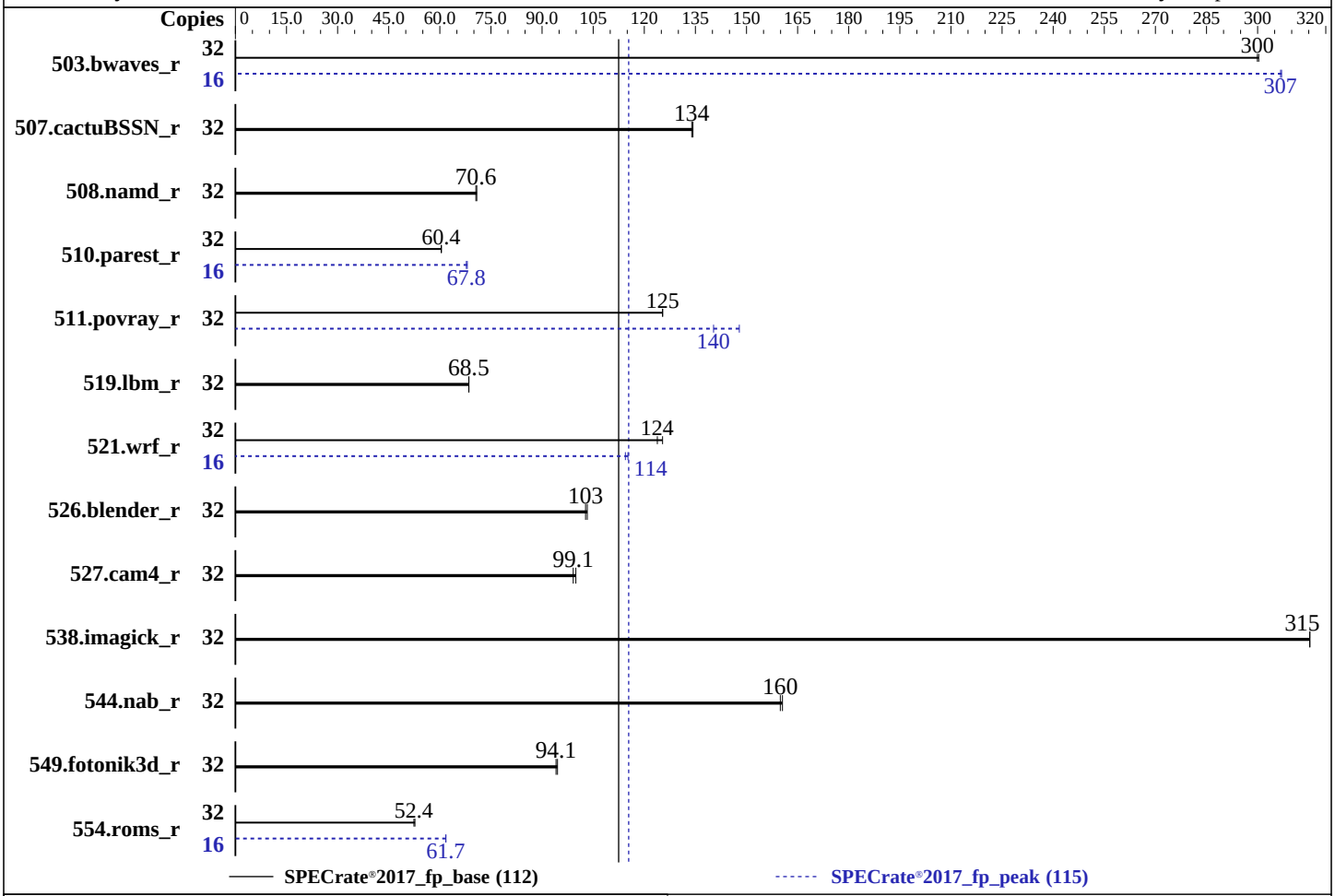
PowerEdge M640 (Intel Xeon Silver 4215R, 3.20 GHz)

SPECrate®2017_fp_base = 112

SPECrate®2017_fp_peak = 115

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Jun-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020



Hardware

CPU Name:	Intel Xeon Silver 4215R
Max MHz:	4000
Nominal:	3200
Enabled:	16 cores, 2 chips, 2 threads/core
Orderable:	1,2 chips
Cache L1:	32 KB I + 32 KB D on chip per core
L2:	1 MB I+D on chip per core
L3:	11 MB I+D on chip per chip
Other:	None
Memory:	384 GB (12 x 32 GB 2Rx8 PC4-2933V-R, running at 2400)
Storage:	1 x 960 GB SATA SSD
Other:	None

Software

OS:	Red Hat Enterprise Linux 8.1 kernel 4.18.0-147.el8.x86_64
Compiler:	C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux; Fortran: Version 19.1.1.217 of Intel Fortran Compiler for Linux
Parallel:	No
Firmware:	Version 2.6.3 released Feb-2020
File System:	tmpfs
System State:	Run level 3 (multi-user)
Base Pointers:	64-bit
Peak Pointers:	64-bit
Other:	None jemalloc memory allocator V5.0.1
Power Management:	BIOS set to prefer performance at the cost of additional power usage.

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Results Table

Benchmark	Base							Peak						
	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Copies	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
503.bwaves_r	32	**1070**	**300**	1069	300			16	523	307	**523**	**307**		
507.cactuBSSN_r	32	**302**	**134**	302	134			32	**302**	**134**	302	134		
508.namd_r	32	429	70.8	**431**	**70.6**			32	429	70.8	**431**	**70.6**		
510.parest_r	32	1384	60.5	**1386**	**60.4**			16	615	68.1	**618**	**67.8**		
511.povray_r	32	596	125	**596**	**125**			32	**532**	**140**	505	148		
519.lbm_r	32	492	68.5	**492**	**68.5**			32	492	68.5	**492**	**68.5**		
521.wrf_r	32	572	125	**579**	**124**			16	**313**	**114**	311	115		
526.blender_r	32	472	103	**474**	**103**			32	472	103	**474**	**103**		
527.cam4_r	32	560	99.9	**565**	**99.1**			32	560	99.9	**565**	**99.1**		
538.imagick_r	32	252	315	**252**	**315**			32	252	315	**252**	**315**		
544.nab_r	32	335	161	**337**	**160**			32	335	161	**337**	**160**		
549.fotonik3d_r	32	1319	94.5	**1325**	**94.1**			32	1319	94.5	**1325**	**94.1**		
554.roms_r	32	965	52.7	**970**	**52.4**			16	411	61.8	**412**	**61.7**		

SPECrate®2017_fp_base = 112

SPECrate®2017_fp_peak = 115

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

```
The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler.
The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
```

Submit Notes

```
The numactl mechanism was used to bind copies to processors. The config file option 'submit'
was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.
```

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
     "/dev/shm/cpu2017-ic19.1u1/lib/intel64:/dev/shm/cpu2017-ic19.1u1/je5.0.1
     -64"
MALLOC_CONF = "retain:true"
```

General Notes

```
Binaries compiled on a system with 1x Intel Core i9-9900K CPU + 64GB RAM
memory using Redhat Enterprise Linux 8.0
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>       /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Benchmark run from a 225 GB ramdisk created with the cmd; "mount -t tmpfs -o size=225G tmpfs /mnt/ramdisk"
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
```

Platform Notes

```
BIOS settings:
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub set to standard
Logical Processor enabled
CPU Interconnect Bus Link Power Management disabled
PCI ASPM L1 Link Power Management disabled
UPI Prefetch enabled
LLC Prefetch disabled
Dead Line LLC Alloc enabled
Directory AtoS disabled

Sysinfo program /dev/shm/cpu2017-ic19.1u1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edb1e6e46a485a0011
running on localhost.localdomain Fri Jun  5 17:27:50 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
   https://www.spec.org/cpu2017/Docs/config.html#sysinfo
```

(Continued on next page)

Platform Notes (Continued)

```
From /proc/cpuinfo
   model name : Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
      2  "physical id"s (chips)
      32 "processors"
   cores, siblings (Caution: counting these is hw and system dependent. The following
   excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
      cpu cores : 8
      siblings  : 16
      physical 0: cores 0 1 2 3 4 5 6 7
      physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
     Architecture:        x86_64
     CPU op-mode(s):      32-bit, 64-bit
     Byte Order:          Little Endian
     CPU(s):              32
     On-line CPU(s) list: 0-31
     Thread(s) per core:  2
     Core(s) per socket:  8
     Socket(s):           2
     NUMA node(s):        2
     Vendor ID:           GenuineIntel
     CPU family:          6
     Model:               85
     Model name:          Intel(R) Xeon(R) Silver 4215R CPU @ 3.20GHz
     Stepping:            7
     CPU MHz:             1502.167
     CPU max MHz:         4000.0000
     CPU min MHz:         1000.0000
     BogoMIPS:            6400.00
     Virtualization:      VT-x
     L1d cache:           32K
     L1i cache:           32K
     L2 cache:            1024K
     L3 cache:            11264K
     NUMA node0 CPU(s):   0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30
     NUMA node1 CPU(s):   1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31
     Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
    pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
    lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
    aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
    xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
    avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
    invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi
    flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
    cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
    avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total
```

(Continued on next page)

Platform Notes (Continued)

```
      cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d
      arch_capabilities

  /proc/cpuinfo cache data
     cache size : 11264 KB

  From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30
    node 0 size: 192073 MB
    node 0 free: 191220 MB
    node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31
    node 1 size: 193506 MB
    node 1 free: 184081 MB
    node distances:
    node   0   1
      0:  10  21
      1:  21  10

  From /proc/meminfo
     MemTotal:       394834632 kB
     HugePages_Total:       0
     Hugepagesize:       2048 kB

  From /etc/*release* /etc/*version*
     os-release:
        NAME="Red Hat Enterprise Linux"
        VERSION="8.1 (Ootpa)"
        ID="rhel"
        ID_LIKE="fedora"
        VERSION_ID="8.1"
        PLATFORM_ID="platform:el8"
        PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
        ANSI_COLOR="0;31"
     redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
     system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
     system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

  uname -a:
     Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
     x86_64 x86_64 x86_64 GNU/Linux

  Kernel self-reported vulnerability status:

  CVE-2018-3620 (L1 Terminal Fault):        Not affected
  Microarchitectural Data Sampling:         Not affected
```

(Continued on next page)

Platform Notes (Continued)

```
 CVE-2017-5754 (Meltdown):                 Not affected
 CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                           via prctl and seccomp
 CVE-2017-5753 (Spectre variant 1):        Mitigation: usercopy/swapgs barriers and __user
                                           pointer sanitization
 CVE-2017-5715 (Spectre variant 2):        Mitigation: Enhanced IBRS, IBPB: conditional,
                                           RSB filling

 run-level 3 Jun 5 12:22

 SPEC is set to: /dev/shm/cpu2017-ic19.1u1
    Filesystem     Type   Size  Used Avail Use% Mounted on
    tmpfs          tmpfs  189G  4.2G  185G   3% /dev/shm

 From /sys/devices/virtual/dmi/id
     BIOS:    Dell Inc. 2.6.3 02/03/2020
     Vendor:  Dell Inc.
     Product: PowerEdge M640
     Product Family: PowerEdge

 Additional information from dmidecode follows.  WARNING: Use caution when you interpret
 this section. The 'dmidecode' program reads system data which is "intended to allow
 hardware to be accurately determined", but the intent may not be met, as there are
 frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
   Memory:
     5x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
     4x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
     3x 00AD069D00AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
     4x Not Specified Not Specified

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
                | 544.nab_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
------------------------------------------------------------------------------
```

(Continued on next page)

Compiler Version Notes (Continued)

```
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C          | 511.povray_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C          | 511.povray_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
```

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Compiler Version Notes (Continued)

```
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
                | 554.roms_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 521.wrf_r(peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

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Compiler Version Notes (Continued)

```
==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1
  NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 521.wrf_r(peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.1.1.217 Build 20200306
Copyright (C) 1985-2020 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto
-mfpmath=sse -funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both Fortran and C:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs

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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using both C and C++:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Benchmarks using Fortran, C, and C++:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-fuse-ld=gold -xCORE-AVX512 -Ofast -ffast-math -flto -mfpmath=sse
-funroll-loops -qopt-mem-layout-trans=4 -O3 -ipo -no-prec-div
-qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

519.lbm_r: basepeak = yes

538.imagick_r: basepeak = yes

544.nab_r: basepeak = yes

C++ benchmarks:

508.namd_r: basepeak = yes

510.parest_r: -m64 -qnextgen
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -Ofast
-ffast-math -flto -mfpmath=sse -funroll-loops
-qopt-mem-layout-trans=4 -L/usr/local/jemalloc64-5.0.1/lib
-ljemalloc

Fortran benchmarks:

503.bwaves_r: -m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -fuse-ld=gold -xCORE-AVX512 -O3 -ipo
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs
-align array32byte -auto -mbranches-within-32B-boundaries
-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc

549.fotonik3d_r: basepeak = yes

554.roms_r: Same as 503.bwaves_r

Benchmarks using both Fortran and C:

521.wrf_r: -prof-gen(pass 1) -prof-use(pass 2) -xCORE-AVX512 -O3
-ipo -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-multiple-gather-scatter-by-shuffles
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-nostandard-realloc-lhs -align array32byte -auto

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Peak Optimization Flags (Continued)

521.wrf_r (continued):
`-L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

527.cam4_r: `basepeak = yes`

Benchmarks using both C and C++:

511.povray_r: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-multiple-gather-scatter-by-shuffles -qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries -L/usr/local/jemalloc64-5.0.1/lib -ljemalloc`

526.blender_r: `basepeak = yes`

Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: `basepeak = yes`

The flags files that were used to format this result can be browsed at
`http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.html`
`http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE10.html`

You can also download the XML flags sources by saving the following links:
`http://www.spec.org/cpu2017/flags/Intel-ic19.1u1-official-linux64_revA.xml`
`http://www.spec.org/cpu2017/flags/Dell-Platform-Flags-PowerEdge-revE10.xml`

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-06-05 17:27:50-0400.
Report generated on 2020-06-23 18:04:47 by CPU2017 PS formatter v6255.
Originally published on 2020-06-23.