# SPEC CPU®2017 Integer Rate Result

## Dell Inc.

PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 55</th>
<th>Test Date: May-2020</th>
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### SPECrate®2017_int_base = 128

### SPECrate®2017_int_peak = 132

- **500.perlbench_r** 40
- **502.gcc_r** 40
- **505.mcf_r** 40
- **520.omnetpp_r** 40
- **523.xalancbmk_r** 40
- **525.x264_r** 40
- **531.deepsjeng_r** 40
- **541.leela_r** 40
- **548.exchange2_r** 40
- **557.xz_r** 40

### Hardware

- **CPU Name:** Intel Xeon Silver 4210R
- **Max MHz:** 3200
- **Nominal:** 2400
- **Enabled:** 20 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 13.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 384 GB (12 x 32 GB 2Rx8 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 480 GB SATA SSD
- **Other:** None

### Software

- **OS:** Red Hat Enterprise Linux 8.1
- **kernel 4.18.0-147.el8.x86_64**
- **Compiler:** C/C++: Version 19.1.1.217 of Intel C/C++ Compiler for Linux;
- **Fortran:** Version 19.1.1.217 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 2.6.3 released Feb-2020
- **File System:** ext4
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
Dell Inc.

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SPEC CPU®2017 Integer Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 128
SPECrate®2017_int_peak = 132

Dell Inc.

GHz)

SPECrate

SPECrate

Results Table

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<td>567</td>
<td>76.2</td>
<td>567</td>
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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Compiler Notes

The inconsistent Compiler version information under Compiler Version section is due to a discrepancy in Intel Compiler. The correct version of C/C++ compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux
The correct version of Fortran compiler is: Version 19.1.1.217 Build 20200306 Compiler for Linux

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:

LD_LIBRARY_PATH = 
"/root/cpu2017-ic19.1u1/lib/intel64:/root/cpu2017-ic19.1u1/lib/ia32:/root/cpu2017-ic19.1u1/jes5.0.1-32"

MALLOC_CONF = "retain:true"
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PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

SPECrate®2017_int_base = 128
SPECrate®2017_int_peak = 132

CPU2017 License: 55
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Tested by: Dell Inc.
Test Date: May-2020
Hardware Availability: Feb-2020
Software Availability: Apr-2020

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numacll i.e.:
numacll --interleave=all runcpu <etc>
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS settings:
Virtualization Technology disabled
DCU Streamer Prefetcher disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub disabled
Logical Processor enabled
CPU Interconnect Bus Link Power Management enabled
PCI ASPM L1 Link Power Management enabled

Sysinfo program /root/cpu2017-ic19.1u1/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble5e46a485a0011
running on localhost.localdomain Wed May 20 16:41:31 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
 model name : Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
 2 "physical id"s (chips)
 40 "processors"

(Continued on next page)
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Platform Notes (Continued)

cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 1000.028
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38
NUMA node1 CPU(s): 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39
Flags:
  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
  lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
  aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
  xtr Newspaper pdcm pcl cid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
  xsave avx f16c rdrand lahf_lm abtm 3nowprefetch cpuid_fault epb cat_l3 cdp_l3
  invpcid_single intel_puin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmmi
  flexpriority ept vpid fsgsbase tsc_adjust bm1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
  avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occmap_llc cqm_mbb_total
  cqm_mbb_local dtc therm ida arat pln pts pkp ospke avx512_vnni md_clear flush_l1d
  arch_capabilities

(Continued on next page)
Dell Inc.

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**Platform Notes (Continued)**

- cache size: 14080 KB

- From `numactl --hardware` **WARNING:** a `numactl 'node'` might or might not correspond to a physical chip.
  - available: 2 nodes (0-1)
  - node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38
  - node 0 size: 192073 MB
  - node 0 free: 172027 MB
  - node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39
  - node 1 size: 193505 MB
  - node 1 free: 147756 MB
  - node distances:
    - node 0: 10 21
    - node 1: 21 10

- From `/proc/meminfo`:
  - MemTotal: 394833124 kB
  - HugePages_Total: 0
  - Hugepagesize: 2048 kB

- From `/etc/*release*` /`etc/*version*`:
  - `os-release`:
    - NAME="Red Hat Enterprise Linux"
    - VERSION="8.1 (Ootpa)"
    - ID="rhel"
    - ID_LIKE="fedora"
    - VERSION_ID="8.1"
    - PLATFORM_ID="platform:el8"
    - PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
    - ANSI_COLOR="0;31"
  - redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
  - system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
  - system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga

- `uname -a`:
  - Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
  - x86_64 x86_64 x86_64 GNU/Linux

- Kernel self-reported vulnerability status:
  - CVE-2018-3620 (L1 Terminal Fault): Not affected
  - Microarchitectural Data Sampling: Not affected
  - CVE-2017-5754 (Meltdown): Not affected
  - CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
  - CVE-2017-5753 (Spectre variant 1): Mitigation: usercopy/swapgs barriers and __user

(Continued on next page)
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**Platform Notes (Continued)**

**pointer sanitation**

Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

---

- **run-level 3 May 15 14:10**
- **SPEC is set to: /root/cpu2017-ic19.1u1**
- **Filesystem**  
  - **Type**  
  - **Size**  
  - **Used**  
  - **Avail**  
  - **Use%**  
  - **Mounted on**

- **/dev/sda2**  
  - ext4 439G 24G 394G 6% /

- **From /sys/devices/virtual/dmi/id**
  - **BIOS:** Dell Inc. 2.6.3 02/03/2020
  - **Vendor:** Dell Inc.
  - **Product:** PowerEdge M640
  - **Product Family:** PowerEdge

---

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

---

**Memory:**

- **5x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933**
- **4x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933**
- **3x 00AD069D00AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933**
- **4x Not Specified Not Specified**

---

(End of data from sysinfo program)

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**Compiler Version Notes**

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Intel(R) C Compiler for applications running on IA-32, Version 2021.1 NextGen Build 20200304

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Intel(R) C Compiler for applications running on Intel(R) 64, Version 2021.1 NextGen Build 20200304

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PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)

**Compiler Version Notes (Continued)**

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```
NextGen Build 20200304
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C       | 500.perlbench_r(peak) 557.xz_r(peak)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base, peak) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
Intel(R) C++ Compiler for applications running on Intel(R) 64, Version 2021.1  
NextGen Build 20200304  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.

Fortran  | 548.exchange2_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)  
64, Version 19.1.1.217 Build 20200306  
Copyright (C) 1985-2020 Intel Corporation. All rights reserved.
```

## Base Compiler Invocation

**C benchmarks:**  
icc

**C++ benchmarks:**  
icpc

**Fortran benchmarks:**  
ifort

## Base Portability Flags

500.perlbench_r: -DSPEC_LP64  -DSPEC_LINUX_X64

(Continued on next page)
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Base Portability Flags (Continued)

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505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -qnextgen -std=c11
-Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse -funroll-loops
-fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

C++ benchmarks:
-m64 -qnextgen -Wl,-plugin-opt=-x86-branches-within-32B-boundaries
-Wl,-z,muldefs -xCORE-AVX512 -O3 -ffast-math -flto -mfpmath=sse
-funroll-loops -fuse-ld=gold -qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Fortran benchmarks:
-m64 -Wl,-plugin-opt=-x86-branches-within-32B-boundaries -Wl,-z,muldefs
-xCORE-AVX512 -O3 -ipo -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs -align array32byte -auto
-mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

(Continued on next page)
### Peak Compiler Invocation (Continued)

Fortran benchmarks:
- `ifort`

### Peak Portability Flags

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<td>502.gcc_r</td>
<td>-D_FILE_OFFSET_BITS=64</td>
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<td>505.mcf_r</td>
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<td>548.exchange2_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

### Peak Optimization Flags

C benchmarks:
- `505.mcf_r`: `basepeak = yes`

(Continued on next page)
# Dell Inc.

**PowerEdge M640 (Intel Xeon Silver 4210R, 2.40 GHz)**

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
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<tbody>
<tr>
<td>128</td>
<td>132</td>
</tr>
</tbody>
</table>

## CPU2017 License: 55

**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  
**Test Date:** May-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** Apr-2020

## Peak Optimization Flags (Continued)

```bash
525.x264_r: -m64 -qnextgen -std=c11
-W1,-plugin-opt=-x86-branches-within-32B-boundaries
-W1,-z,muldefs -xCORE-AVX512 -flto -O3 -ffast-math
-fuse-ld=gold -qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc

557.xz_r: -W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -mbranches-within-32B-boundaries
-L/usr/local/IntelCompiler19/compilers_and_libraries_2020.1.217/linux/compiler/lib/intel64_lin
-lqkmalloc
```

### C++ benchmarks:

- `520.omnetpp_r`: basepeak = yes
- `523.xalancbmk_r`: basepeak = yes
- `531.deepsjeng_r`: basepeak = yes
- `541.leela_r`: basepeak = yes

### Fortran benchmarks:

- `548.exchange2_r`: basepeak = yes

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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