# SPEC CPU®2017 Floating Point Rate Result

## Inspur Corporation

**Inspur NF5280M5 (Intel Xeon Silver 4214)**

**SPECrate®2017_fp_base = 139**

**SPECrate®2017_fp_peak = 146**

### CPU2017 License: 3358

**Test Sponsor:** Inspur Corporation  
**Tested by:** Inspur Corporation

**Test Date:** Apr-2020  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Hardware

| Copies | 0 | 20 | 40 | 60 | 80 | 100 | 120 | 140 | 160 | 180 | 200 | 220 | 240 | 260 | 280 | 300 | 320 | 340 | 360 | 380 | 400 |
|--------|---|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 503.bwaves_r | 48 | 109 | 109 |
| 507.cactuBSSN_r | 48 | 95.2 | 94.5 |
| 508.namd_r | 48 | 82.7 | 95.2 |
| 510.parest_r | 24 | 147 | 147 |
| 511.povray_r | 48 | 88.4 | 94.1 |
| 519.lbm_r | 48 | 153 | 153 |
| 521.wrf_r | 24 | 139 | 139 |
| 526.blender_r | 48 | 138 | 138 |
| 527.cam4_r | 48 | 144 | 144 |
| 538.imagick_r | 48 | 290 | 290 |
| 544.nab_r | 48 | 211 | 211 |
| 549.fotonik3d_r | 48 | 125 | 125 |
| 554.roms_r | 24 | 88.8 | 88.8 |

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base (139)</th>
<th>SPECrate®2017_fp_peak (146)</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
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</tr>
</tbody>
</table>

### Software

**OS:** SUSE Linux Enterprise Server 12 SP4 4.12.14-94.41-default

**Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux

**Parallel:** No

**Firmware:** Version 4.1.7 released Apr-2019

**File System:** xfs

**System State:** Run level 3 (multi-user)

**Base Pointers:** 64-bit

**Peak Pointers:** 64-bit

**Other:** None

**Power Management:** BIOS and OS set to prefer performance at the cost of additional power usage.

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**CPU Name:** Intel Xeon Silver 4214

**Max MHz:** 3200

**Nominal:** 2200

**Enabled:** 24 cores, 2 chips, 2 threads/core

**Orderable:** 1,2 chips

**Cache L1:** 32 KB I + 32 KB D on chip per core

**L2:** 1 MB I+D on chip per core

**L3:** 16.5 MB I+D on chip per chip

**Other:** None

**Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)

**Storage:** 1 x 2 TB NVME SSD

**Other:** None

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**Page 1**

Standard Performance Evaluation Corporation (info@spec.org)  
https://www.spec.org/
Inspur Corporation

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Results Table

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<tr>
<th>Benchmark</th>
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<td>429</td>
<td>88.8</td>
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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
SCALEING_GOVERNOR set to Performance

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/CPU2017/lib/intel64"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
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| SPECrate®2017_fp_base = 139 |
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**CPU2017 License:** 3358
**Test Sponsor:** Inspur Corporation
**Tested by:** Inspur Corporation

**Test Date:** Apr-2020
**Hardware Availability:** Apr-2019
**Software Availability:** May-2019

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### General Notes (Continued)

- **runcpu command invoked through numactl i.e.:**
  numactl --interleave=all runcpu <etc>

- **NA:** The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
- **Yes:** The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
- **Yes:** The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

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### Platform Notes

**BIOS configuration:**
ENERGY_PERF_BIAS_CFG mode set to Performance
Hardware Prefetch set to Disable
VT Support set to Disable
C1E Support set to Disable
IMC (Integrated memory controller) Interleaving set to 2-way
Sub NUMA Cluster (SNC) set to Disable

**Sysinfo program** /home/CPU2017/bin/sysinfo
**Rev:** r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
**Running on** linux-nlir Tue Apr 28 19:24:29 2020

**SUT (System Under Test) info as seen by some common utilities.**
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

- **From /proc/cpuinfo**
  - model name : Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
  - 2 "physical id" s (chips)
  - 48 "processors"
  - cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    - cpu cores : 12
    - siblings : 24
    - physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
    - physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

- **From lscpu:**
  - Architecture: x86_64
  - CPU op-mode(s): 32-bit, 64-bit
  - Byte Order: Little Endian
  - CPU(s): 48
  - On-line CPU(s) list: 0-47

(Continued on next page)
## Platform Notes (Continued)

- Thread(s) per core: 2
- Core(s) per socket: 12
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85
- Model name: Intel(R) Xeon(R) Silver 4214 CPU @ 2.20GHz
- Stepping: 6
- CPU MHz: 2200.000
- CPU max MHz: 3200.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 4400.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 16896K
- NUMA node0 CPU(s): 0-11,24-35
- NUMA node1 CPU(s): 12-23,36-47
- Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx mdtes64 ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebp cat_l3 cdp_l3 invpcid single ssbd mba ibrs ibpb stibp tpr_shadow vnumi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512v1 xsaveopt xsavec xsaveopt xsavec xsaveprec qc qm qm_tele total qm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni flush_l1d arch_capabilities

From `numactl --hardware` WARNING: a numactl 'node' might or might not correspond to a physical chip.
- available: 2 nodes (0-1)
- node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 24 25 26 27 28 29 30 31 32 33 34 35
- node 0 size: 385579 MB
- node 0 free: 371579 MB
- node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23 24 37 38 39 40 41 42 43 44 45 46 47
- node 1 size: 386820 MB
- node 1 free: 375348 MB
- node distances:
  - node 0: 10 21

(Continued on next page)
Platform Notes (Continued)

1:  21 10

From /proc/meminfo
   MemTotal:       790938204 kB
   HugePages_Total:       0
   Hugepagesize:       2048 kB

/usr/bin/lsb_release -d
   SUSE Linux Enterprise Server 12 SP4

From /etc/*release* /etc/*version*
   SuSE-release:
      SUSE Linux Enterprise Server 12 (x86_64)
      VERSION = 12
      PATCHLEVEL = 4
      # This file is deprecated and will be removed in a future service pack or release.
      # Please check /etc/os-release for details about this release.
      os-release:
         NAME="SLES"
         VERSION="12-SP4"
         VERSION_ID="12.4"
         PRETTY_NAME="SUSE Linux Enterprise Server 12 SP4"
         ID="sles"
         ANSI_COLOR="0;32"
         CPE_NAME="cpe:/o:suse:sles:12:sp4"

   uname -a:
      x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Apr 28 10:02 last=5

SPEC is set to: /home/CPU2017
   Filesystem  Type  Size  Used Avail Use% Mounted on
   /dev/nvme0n1p4 xfs 1.8T  50G  1.8T  3% /home

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**Platform Notes (Continued)**

From /sys/devices/virtual/dmi/id

BIOS: American Megatrends Inc. 4.1.7 04/19/2019
Vendor: Inspur
Product: NF5280M5
Serial: 219243921

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
24x Samsung M393A4K40CB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

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**Compiler Version Notes**

```
| C       | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak) |

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
| C++     | 508.namd_r(base, peak) 510.parest_r(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
| C++, C   | 511.povray_r(base, peak) 526.blender_r(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
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```

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Compiler Version Notes (Continued)

C++, C, Fortran | 507.cactuBSSN_r(base, peak)

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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
         | 554.roms_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
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Fortran, C | 521.wrf_r(base, peak) 527.cam4_r(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

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**Base Compiler Invocation (Continued)**

Benchmarks using both C and C++:

```bash
icpc -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:

```bash
icpc -m64 icc -m64 -std=c11 ifort -m64
```

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**Base Portability Flags**

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

---

**Base Optimization Flags**

**C benchmarks:**

```bash
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4
```

**C++ benchmarks:**

```bash
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4
```

**Fortran benchmarks:**

```bash
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte
```

**Benchmarks using both Fortran and C:**

```bash
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
```

(Continued on next page)
Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
-align array32byte

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

(Continued on next page)
Inspur Corporation
Inspur NF5280M5 (Intel Xeon Silver 4214)

Peak Optimization Flags (Continued)

519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 
-no-prec-div -qopt-prefetch -ffinite-math-only 
-qopt-mem-layout-trans=4

538.imagick_r: -ipo -O3 -no-prec-div -qopt-prefetch 
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 
-no-prec-div -qopt-prefetch -ffinite-math-only 
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch 
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch 
-ffinite-math-only -qopt-mem-layout-trans=4 -auto 
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 
-no-prec-div -qopt-prefetch -ffinite-math-only 
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs 
-align array32byte

Benmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 
-no-prec-div -qopt-prefetch -ffinite-math-only 
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs 
-align array32byte

Benmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3 
-no-prec-div -qopt-prefetch -ffinite-math-only 
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch 
-ffinite-math-only -qopt-mem-layout-trans=4
## SPEC CPU®2017 Floating Point Rate Result

**Inspur Corporation**

**Inspur NF5280M5 (Intel Xeon Silver 4214)**

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<td>Hardware Availability</td>
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### SPECrate®2017_fp_base = 139

### SPECrate®2017_fp_peak = 146

#### Benchmarks using Fortran, C, and C++:

- `-xCORE-AVX2`
- `-ipo`
- `-O3`
- `-no-prec-div`
- `-qopt-prefetch`
- `-ffinite-math-only`
- `-qopt-mem-layout-trans=4`
- `-auto`
- `-nostandard-realloc-lhs`
- `-align array32byte`

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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Tested with SPEC CPU®2017 v1.1.0 on 2020-04-28 07:24:29-0400.