### Dell Inc. PowerEdge T440 (Intel Xeon Silver 4209T, 2.20 GHz)

**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  

**Copies**

<table>
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<tr>
<th>Benchmark</th>
<th>Copies</th>
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**Hardware**

- **CPU Name:** Intel Xeon Silver 4209T  
- **Max MHz:** 3200  
- **Nominal:** 2200  
- **Enabled:** 32 cores, 2 chips  
- **Orderable:** 1,2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 11 MB I+D on chip per core  
- **Memory:** 384 GB (12 x 32 GB 2Rx8 PC4-2933V-R, running at 2933)  
- **Storage:** 1 x 1.92 TB SATA SSD  
- **Other:** None

**Software**

- **OS:** Red Hat Enterprise Linux 8.1  
- **Compiler:** C/C++: Version 19.0.5.281 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.5.281 of Intel Fortran Compiler for Linux  
- **Parallel:** No  
- **Firmware:** Version 2.5.4 released Jan-2020  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** None  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
### Dell Inc.

**PowerEdge T440 (Intel Xeon Silver 4209T, 2.20 GHz)**

**SPEC CPU®2017 Floating Point Rate Result**

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</table>

**SPECrate®2017_fp_base = 89.5**

**SPECrate®2017_fp_peak = 92.8**

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### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- MALLOC_CONF = "retain:true"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-9900K CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)

(Continued on next page)
Dell Inc.  

PowerEdge T440 (Intel Xeon Silver 4209T, 2.20 GHz)  

---

General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numacll i.e.:
numactl --interleave=all runcpu <etc>

---

Platform Notes

BIOS settings:
Virtualization Technology disabled
System Profile set to Custom
CPU Performance set to Maximum Performance
C States set to Autonomous
C1E disabled
Uncore Frequency set to Dynamic
Energy Efficiency Policy set to Performance
Memory Patrol Scrub disabled
Logical Processor disabled
CPU Interconnect Bus Link Power Management disabled
PCI ASPM L1 Link Power Management disabled
UPI Prefetch enabled
LLC Prefetch disabled
Dead Line LLC Alloc enabled
Directory AtoS disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
running on localhost.localdomain Sun Apr 26 03:28:11 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

    model name : Intel(R) Xeon(R) Silver 4209T CPU @ 2.20GHz
        2 "physical id"s (chips)
        32 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 8
    siblings : 16
    physical 0: cores 0 1 2 3 4 5 6 7

(Continued on next page)
Dell Inc. PowerEdge T440 (Intel Xeon Silver 4209T, 2.20 GHz)

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

SPECRate®2017_fp_base = 89.5
SPECRate®2017_fp_peak = 92.8

Platform Notes (Continued)

physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 32
On-line CPU(s) list: 0-31
Thread(s) per core: 2
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4209T CPU @ 2.20GHz
Stepping: 6
CPU MHz: 1510.074
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30
NUMA node1 CPU(s): 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pni ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erva invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsavegs cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

/proc/cpuinfo cache data
cache size : 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)

(Continued on next page)
## Dell Inc. PowerEdge T440 (Intel Xeon Silver 4209T, 2.20 GHz)

**SPECrate®2017_fp_base = 89.5**  
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<td>Test Date:</td>
<td>Apr-2020</td>
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<td>Hardware Availability:</td>
<td>Feb-2020</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Nov-2019</td>
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</table>

### Platform Notes (Continued)

```
node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30
node 0 size: 192049 MB
node 0 free: 190813 MB
node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31
node 1 size: 193532 MB
node 1 free: 192010 MB
node distances:
  node 0 1
  0: 10 21
  1: 21 10
```

From `/proc/meminfo`

```
MemTotal:       394835328 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
```

From `/etc/*release* /etc/*version*`

```
os-release:
  NAME="Red Hat Enterprise Linux"
  VERSION="8.1 (Ootpa)"
  ID="rhel"
  ID_LIKE="fedora"
  VERSION_ID="8.1"
  PLATFORM_ID="platform:el8"
  PRETTY_NAME="Red Hat Enterprise Linux 8.1 (Ootpa)"
  ANSI_COLOR="0;31"
redhat-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release: Red Hat Enterprise Linux release 8.1 (Ootpa)
system-release-cpe: cpe:/o:redhat:enterprise_linux:8.1:ga
```

```
uname -a:
Linux localhost.localdomain 4.18.0-147.el8.x86_64 #1 SMP Thu Sep 26 15:52:44 UTC 2019
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- **CVE-2018-3620 (L1 Terminal Fault):** Not affected
- **Microarchitectural Data Sampling:** Not affected
- **CVE-2017-5754 (Meltdown):** Not affected
- **CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- **CVE-2017-5753 (Spectre variant 1):** Mitigation: usercopy/swapgs barriers and __user pointer sanitization
- **CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

```
run-level 3 Apr 25 20:35 last=5
```

(Continued on next page)
Dell Inc. PowerEdge T440 (Intel Xeon Silver 4209T, 2.20 GHz) SPECrate®2017_fp_base = 89.5
SPECrate®2017_fp_peak = 92.8

Platform Notes (Continued)

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/mapper/rhel-home xfs 1.7T 20G 1.7T 2% /home

From /sys/devices/virtual/dmi/id
BIOS: Dell Inc. 2.5.4 01/14/2020
Vendor: Dell Inc.
Product: PowerEdge T440
Product Family: PowerEdge
Serial: FBLH613

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
4x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
8x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
4x Not Specified Not Specified

(End of data from sysinfo program)

Compiler Version Notes

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Test Date: Apr-2020
Hardware Availability: Feb-2020
Software Availability: Nov-2019

Compiler Version Notes (Continued)

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Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64,
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C++, C, Fortran | 507.cactuBSSN_r(base, peak)
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Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64,
  Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R)
  64, Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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Fortran | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
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Base Compiler Invocation

C benchmarks:
  icc

(Continued on next page)
Base Compiler Invocation (Continued)

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.llm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-m64 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
Dell Inc.

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CPU2017 License: 55
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Base Optimization Flags (Continued)

Fortran benchmarks:
-m64 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Benchmarks using both C and C++:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort
### Dell Inc.

**PowerEdge T440 (Intel Xeon Silver 4209T, 2.20 GHz)**

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>= 89.5</th>
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<tr>
<td>SPECrate®2017_fp_peak</td>
<td>= 92.8</td>
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</table>

**CPU2017 License:** 55

**Test Date:** Apr-2020

**Test Sponsor:** Dell Inc.

**Hardware Availability:** Feb-2020

**Tested by:** Dell Inc.

**Software Availability:** Nov-2019

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

**C benchmarks:**

- 519.lbm_r: -m64 -std=c11 -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX2 -03 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=4

- 538.imagick_r: basepeak = yes

- 544.nab_r: basepeak = yes

**C++ benchmarks:**

- 508.namd_r: -m64 -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX2 -03 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=4

- 510.parest_r: -m64 -xCORE-AVX2 -ipo -03 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=4

**Fortran benchmarks:**

- 503.bwaves_r: -m64 -xCORE-AVX2 -ipo -03 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=4 -auto
  -nostandard-realloc-lhs

- 549.fotonik3d_r: basepeak = yes

- 554.roms_r: -m64 -prof-gen(pass 1) -prof-use(pass 2) -ipo
  -xCORE-AVX2 -03 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=4 -auto
  -nostandard-realloc-lhs

**Benchmarks using both Fortran and C:**

- -m64 -std=c11 -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2
  -03 -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs

**Benchmarks using both C and C++:**

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

**Dell Inc.**

### PowerEdge T440 (Intel Xeon Silver 4209T, 2.20 GHz)

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### Peak Optimization Flags (Continued)

```bash
511.povray_r: -m64 -std=c11 -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX2 -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

526.blender_r: basepeak = yes

### Benchmarks using Fortran, C, and C++:

507.cactuBSSN_r: basepeak = yes

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-04-26 04:28:11-0400.
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