Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242R, 3.10GHz)

<table>
<thead>
<tr>
<th>Program</th>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<tbody>
<tr>
<td>503.bwaves_r</td>
<td>80</td>
<td>200</td>
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<tr>
<td>507.cactuBSSN_r</td>
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<td>508.namd_r</td>
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<tr>
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<td>511.povray_r</td>
<td>80</td>
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<td>519.lbm_r</td>
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<tr>
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<tr>
<td>554.roms_r</td>
<td>80</td>
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</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6242R
- **Max MHz:** 4100
- **Nominal:** 3100
- **Enabled:** 40 cores, 2 chips, 2 threads/core
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 35.75 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 240 GB SSD SAS

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4b released Apr-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242R, 3.10GHz)

SPEC CPU®2017 Floating Point Rate Result

Copyright 2017-2020 Standard Performance Evaluation Corporation

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed81e6e46a485a0011
running on linux-5vrl Thu Apr 16 10:25:00 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 5 6 10 11 12 13 16 17 18 19 21 24 26 27 28 29
physical 1: cores 0 1 2 3 5 6 9 10 12 13 16 17 18 19 20 21 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4

SPECrate®2017_fp_base = 248
SPECrate®2017_fp_peak = 253
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242R, 3.10GHz)  

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  

SPECrate®2017_fp_base = 248  
SPECrate®2017_fp_peak = 253  

Test Date: Apr-2020  
Hardware Availability: Feb-2020  
Software Availability: May-2019

Platform Notes (Continued)

Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz
Stepping:            7
CPU MHz:             3100.000
CPU max MHz:         4100.0000
CPU min MHz:         1200.0000
BogoMIPS:            6200.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            36608K
NUMA node0 CPU(s):   0-3, 6, 10-12, 15, 16, 40-43, 46-50, 52, 55, 56
NUMA node1 CPU(s):   4, 5, 7-9, 13, 14, 17-19, 44, 45, 47-49, 53, 54, 57-59
NUMA node2 CPU(s):   20-23, 26, 27, 30-32, 36, 60-63, 66, 67, 70-72, 76
NUMA node3 CPU(s):   24, 25, 28, 29, 33-35, 37-39, 64, 65, 68, 69, 73-75, 77-79
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmerge tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdmb fma cx16 xptr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdip_l3 invpcid_single intel_pchin mba tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrms invpcid rtm cmmp mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves xsavec xgetbv1 xsaves cmqm_llc cmqm_occuq_llc cmqm_mbm_total cmqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
n0 node 0 cpus: 0 1 2 3 6 10 11 12 15 16 40 41 42 43 46 50 51 52 55 56
node 0 size: 192061 MB
node 0 free: 191102 MB
node 1 cpus: 4 5 7 8 9 13 14 17 18 19 44 45 47 48 49 53 54 57 58 59
node 1 size: 193521 MB
node 1 free: 192857 MB
node 2 cpus: 20 21 22 23 26 27 30 31 32 36 60 61 62 63 66 67 70 71 72 76
node 2 size: 193521 MB
node 2 free: 192882 MB
node 3 cpus: 24 25 28 29 33 34 35 37 38 39 64 65 68 69 73 74 75 77 78 79

(Continued on next page)
## Platform Notes (Continued)

node 3 size: 193519 MB  
node 3 free: 192940 MB  
node distances:  
node  0  1  2  3  
  0: 10 11 21 21  
  1: 11 10 21 21  
  2: 21 21 10 11  
  3: 21 21 11 10  

From /proc/meminfo  
MemTotal: 791167584 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB  

From /etc/*release* /etc/*version*  
  os-release:  
    NAME="SLES"  
    VERSION="15"  
    VERSION_ID="15"  
    PRETTY_NAME="SUSE Linux Enterprise Server 15"  
    ID="sles"  
    ID_LIKE="suse"  
    ANSI_COLOR="0;32"  
    CPE_NAME="cpe:/o:suse:sles:15"  

uname -a:  
Linux linux-5vrl 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)  
x86_64 x86_64 x86_64 GNU/Linux  

Kernel self-reported vulnerability status:  
CVE-2018-3620 (L1 Terminal Fault): No status reported  
Microarchitectural Data Sampling: No status reported  
CVE-2017-5754 (Meltdown): Not affected  
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled  
via prctl and seccomp  
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted  
Speculation, IBPB, IBRS_FW  

run-level 3 Apr 15 21:27  
SPEC is set to: /home/cpu2017  
  Filesystem Type Size Used Avail Use% Mounted on  
  /dev/sdb1 btrfs 224G 31G 193G 14% /home  

From /sys/devices/virtual/dmi/id

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242R, 3.10GHz)

SPECrate®2017_fp_base = 248
SPECrate®2017_fp_peak = 253

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

BIOS: Cisco Systems, Inc. B200M5.4.0.4b.0.0.0407191258 04/07/2019
Vendor: Cisco Systems Inc
Product: UCSB-B200-M5
Serial: FCH22237D2V

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

C++             | 508.namd_r(base, peak) 510.parest_r(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

C++, C, Fortran | 507.cactuBSSN_r(base, peak)
(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242R, 3.10GHz)

SPECrate®2017_fp_base = 248
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Fortran
503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak)
554.roms_r(base, peak)

Fortran, C
521.wrf_r(base, peak) 527.cam4_r(base, peak)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242R, 3.10GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Base Compiler Invocation ( Continued )

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactusBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch
-ffinite-math-only -gopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Apr-2020
Tested by: Cisco Systems
Hardware Availability: Feb-2020
Software Availability: May-2019

Base Optimization Flags (Continued)

Benchmarks using both C and C++:
  -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
  -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
  -ffinite-math-only -qopt-mem-layout-trans=4 -auto
  -nostandard-realloc-lhs -align array32byte

Peak Compiler Invocation

C benchmarks:
  icc -m64 -std=c11

C++ benchmarks:
  icpc -m64

Fortran benchmarks:
  ifort -m64

Benchmarks using both Fortran and C:
  ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
  icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
  icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
  519.lbm_r -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
  -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
  -qopt-mem-layout-trans=4

(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Peak Optimization Flags (Continued)

538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -03
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-03 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6242R, 3.10GHz)

SPECrate®2017_fp_base = 248
SPECrate®2017_fp_peak = 253

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Apr-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revK.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-04-16 13:24:59-0400.
Originally published on 2020-05-12.