Lenovo Global Technology
ThinkSystem SR630
(2.40 GHz, Intel Xeon Silver 4214R)

**SPEC CPU®2017 Floating Point Rate Result**

<table>
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<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>Hardware Availability</th>
<th>Software Availability</th>
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<tr>
<td>48</td>
<td>145</td>
<td>Apr-2020</td>
<td>Sep-2019</td>
</tr>
</tbody>
</table>

**Test Sponsor:** Lenovo Global Technology

**Test Date:** Apr-2020

**CPU2017 License:** 9017

**Tested by:** Lenovo Global Technology

**Hardware**
- **CPU Name:** Intel Xeon Silver 4214R
- **Max MHz:** 3500
- **Nominal:** 2400
- **Enabled:** 24 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 16.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)
- **Storage:** 1 x 800 GB SATA SSD
- **Other:** None

**Software**
- **OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)
- **Kernel:** 4.12.14-195-default
- **Compiler:**
  - C/C++: Version 19.0.5.281 of Intel C/C++
  - Fortran: Version 19.0.5.281 of Intel Fortran
  - Compiler for Linux
- **Parallel:** No
- **Firmware:**
  - Lenovo BIOS Version IVE152L 2.51 released Feb-2020 tested as IVE151L 2.51 Jan-2020
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
## Lenovo Global Technology

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---

### Results Table

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</tbody>
</table>

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### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017-1.1.0-ic19.0u5/lib/intel64"

---

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
sync; echo 3>/proc/sys/vm/drop_caches  
(Continued on next page)
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General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3640 (Spectre variant 3a) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3639 (Spectre variant 4) is mitigated in the system as tested and documented.

Platform Notes

BIOS configuration:
Choose Operating Mode set to Maximum Performance and then set it to Custom Mode
C-States set to Legacy
SNC set to Enable
DCU Streamer Prefetcher set to Disable
Trusted Execution Technology set to Enable
Stale AtoS set to Enable
LLC dead line alloc set to Disable
Patrol Scrub set to Disable

Sysinfo program /home/cpu2017-1.1.0-ic19.0u5/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edb1e6e46a485a0011
running on linux-thtl Thu Apr  2 21:39:05 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
 2 "physical id"s (chips)
48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 24
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13

From lscpu:
Architecture: x86_64

(Continued on next page)
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Platform Notes (Continued)

CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 2
Core(s) per socket: 12
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4214R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 2400.000
CPU max MHz: 3500.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 16896K
NUMA node0 CPU(s): 0-2, 6-8, 24-26, 30-32
NUMA node1 CPU(s): 3-5, 9-11, 27-29, 33-35
NUMA node2 CPU(s): 12-14, 18-20, 36-38, 42-44
NUMA node3 CPU(s): 15-17, 21-23, 39-41, 45-47
Flags: fpu vme de pse tsc msr pae mce cx8 apt mpx cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrr pdcm pcp dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmci flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrp invpcid rtm cmp mxp rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_l1d arch_capabilities

/proc/cpuinfo cache data
  cache size : 16896 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 6 7 8 24 25 26 30 31 32

(Continued on next page)
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<th>145</th>
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<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
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<tr>
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<th>9017</th>
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<tr>
<td>Test Sponsor:</td>
<td>Lenovo Global Technology</td>
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<td>Tested by:</td>
<td>Lenovo Global Technology</td>
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<td>Mar-2020</td>
</tr>
<tr>
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<td>Sep-2019</td>
</tr>
</tbody>
</table>

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**Platform Notes (Continued)**

```plaintext
node 0 size: 193123 MB  
node 0 free: 192797 MB  
node 1 cpus: 3 4 5 9 10 11 27 28 29 33 34 35  
node 1 size: 193533 MB  
node 1 free: 193209 MB  
node 2 cpus: 12 13 14 18 19 20 36 37 38 42 43 44  
node 2 size: 193533 MB  
node 2 free: 193318 MB  
node 3 cpus: 15 16 17 21 22 23 39 40 41 45 46 47  
node 3 size: 193532 MB  
node 3 free: 193312 MB  
node distances:  
  node 0 1 2 3  
  0: 10 11 21 21  
  1: 11 10 21 21  
  2: 21 21 10 11  
  3: 21 21 11 10  
```

From `/proc/meminfo`

- MemTotal: 792292992 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release*` /`/etc/*version*`

```plaintext
os-release:  
  NAME="SLES"  
  VERSION="15-SP1"  
  VERSION_ID="15.1"  
  PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"  
  ID="sles"  
  ID_LIKE="suse"  
  ANSI_COLOR="0;32"  
  CPE_NAME="cpe:/o:suse:sles:15:sp1"  
```

```plaintext
uname -a:  
  Linux linux-thtl 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)  
  x86_64 x86_64 x86_64 GNU/Linux  
```

Kernel self-reported vulnerability status:

**CVE-2018-3620 (L1 Terminal Fault):** Not affected
**Microarchitectural Data Sampling:** Not affected
**CVE-2017-5754 (Meltdown):** Not affected
**CVE-2018-3639 (Speculative Store Bypass):** Mitigation: Speculative Store Bypass disabled via prctl and seccomp
**CVE-2017-5753 (Spectre variant 1):** Mitigation: __user pointer sanitization
**CVE-2017-5715 (Spectre variant 2):** Mitigation: Enhanced IBRS, IBPB: conditional,
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SPECrater®2017_fp_base = 145
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Test Date: Apr-2020
Hardware Availability: Mar-2020
Software Availability: Sep-2019

Platform Notes (Continued)

RSB filling

run-level 3 Apr 2 21:36

SPEC is set to: /home/cpu2017-1.1.0-ic19.0u5
 Filesystem   Type Size Used Avail Use% Mounted on
 /dev/sdd2     xfs   744G  33G  712G   5% /

From /sys/devices/virtual/dmi/id
 BIOS:  Lenovo -[IVE151L-2.51]- 01/14/2020
 Vendor: Lenovo
 Product: System X -[7X01RCZ000]-
 Product Family: ThinkSystem
 Serial: 1234567890

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x Samsung M393A4K40CB2-CVF 32 GB 2 rank 2933

Compiler Version Notes

==============================================================================
C                | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C++              | 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

==============================================================================
C++, C           | 511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,

(Continued on next page)
Lenovo Global Technology

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SPECrater®2017_fp_base = 145
SPECrater®2017_fp_peak = Not Run

Compiler Version Notes (Continued)

Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64,
Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C, Fortran | 507.cactusBSSN_r(base)

Intel (R) C++ Intel (R) 64 Compiler for applications running on Intel (R) 64,
Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64,
Version 19.0.5.281 Build 20190815
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Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R) 64,
Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)

Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R) 64,
Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran, C | 521.wrf_r(base) 527.cam4_r(base)

Intel (R) Fortran Intel (R) 64 Compiler for applications running on Intel (R) 64,
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Intel (R) C Intel (R) 64 Compiler for applications running on Intel (R) 64,
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Base Compiler Invocation

C benchmarks:
icc

(Continued on next page)
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Base Compiler Invocation (Continued)

C++ benchmarks:
icpc

Fortran benchmarks:
ifort

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

Base Portability Flags

```
503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64
```

Base Optimization Flags

```
C benchmarks:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-m64 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

(Continued on next page)
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Base Optimization Flags (Continued)

Fortran benchmarks:
-m64 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Benchmarks using both C and C++:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-G.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-G.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-04-02 09:39:05-0400.