**Lenovo Global Technology**

**ThinkSystem SR570**

(2.10 GHz, Intel Xeon Gold 5218R)

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**SPECrater®2017_fp_base** = 190  
**SPECrater®2017_fp_peak** = Not Run

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**Hardware**

- CPU Name: Intel Xeon Gold 5218R  
- Max MHz: 4000  
- Nominal: 2100  
- Enabled: 40 cores, 2 chips, 2 threads/core  
- Orderable: 1,2 chips  
- Cache L1: 32 KB I + 32 KB D on chip per core  
- L2: 1 MB I+D on chip per core  
- L3: 27.5 MB I+D on chip per chip  
- Other: None  
- Memory: 192 GB (12 x 16 GB 2Rx8 PC4-2933Y-R, running at 2666)  
- Storage: 1 x 960 GB SATA SSD  
- Other: None

**Software**

- OS: SUSE Linux Enterprise Server 15 SP1 (x86_64)  
- Kernel 4.12.14-195-default  
- Compiler:  
  - C/C++: Version 19.0.5.281 of Intel  
  - C/C++ Compiler for Linux;  
- Fortran: Version 19.0.5.281 of Intel Fortran  
- Compiler for Linux  
- Parallel: No  
- Firmware: Lenovo BIOS Version TEE152L 2.51 released Feb-2020 tested as TEE151L 2.51 Jan-2020  
- File System: xfs  
- System State: Run level 3 (multi-user)  
- Base Pointers: 64-bit  
- Peak Pointers: Not Applicable  
- Other: None  
- Power Management: BIOS set to prefer performance at the cost of additional power usage

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**Test Sponsor:** Lenovo Global Technology  
**Tested by:** Lenovo Global Technology  
**Test Date:** Mar-2020  
**Hardware Availability:** Mar-2020  
**Software Availability:** Sep-2019

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Lenovo Global Technology
ThinkSystem SR570
(2.10 GHz, Intel Xeon Gold 5218R)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Test Date: Mar-2020
Hardware Availability: Mar-2020
Software Availability: Sep-2019

Results Table

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SPECrater®2017_fp_base = 190
SPECrater®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017-1.1.0-ic19.0u5/lib/intel64"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7980XE CPU + 64GB RAM memory using Redhat Enterprise Linux 8.0
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

(Continued on next page)
**General Notes (Continued)**

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3640 (Spectre variant 3a) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3639 (Spectre variant 4) is mitigated in the system as tested and documented.

**Platform Notes**

BIOS configuration:
Choose Operating Mode set to Maximum Performance and then set it to Custom Mode
MONITOR/MWAIT set to Enable
SNC set to Enable

Sysinfo program /home/cpu2017-1.1.0-ic19.0u5/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed6e6e46a485a0011
running on linux-mazt Thu Mar 19 01:09:53 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
```

From lscpu:

```
Architecture:      x86_64
CPU op-mode(s):    32-bit, 64-bit
Byte Order:        Little Endian
Address sizes:     46 bits physical, 48 bits virtual
CPU(s):            80
On-line CPU(s) list: 0-79
```

(Continued on next page)
Platform Notes (Continued)

Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
Stepping: 7
CPU MHz: 2100.000
CPU max MHz: 4000.0000
CPU min MHz: 800.0000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-2,5,6,10-12,15,16,40-42,45,46,50-52,55,56
NUMA node1 CPU(s): 3,4,7-9,13,14,17-19,43,44,47-49,53,54,57-59
NUMA node2 CPU(s): 20-22,25,26,30-32,35,36,60-62,65,66,70-72,75,76
NUMA node3 CPU(s): 23,24,27-29,33,34,37-39,63,64,67-69,73,74,77-79
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vmi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mxp rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total
cqm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld
arch_capabilities

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 4 nodes (0-3)
node 0 cpus: 0 1 2 5 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
node 0 size: 47673 MB
node 0 free: 46651 MB
node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 58 59
node 1 size: 48380 MB
node 1 free: 47913 MB

/proc/cpuinfo cache data
  cache size : 28160 KB

(Continued on next page)
Lenovo Global Technology
ThinkSystem SR570
(2.10 GHz, Intel Xeon Gold 5218R)

| SPECrate®2017_fp_base = | 190 |
| SPECrate®2017_fp_peak = | Not Run |

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

Platform Notes (Continued)

node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
node 2 size: 48380 MB
node 2 free: 47891 MB
node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
node 3 size: 48378 MB
node 3 free: 47926 MB
node distances:
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 197440020 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
os-release:
NAME="SLES"
VERSION="15-SP1"
VERSION_ID="15.1"
PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15:sp1"
uname -a:
Linux linux-mazt 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: ___user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 18 19:52

SPEC is set to: /home/cpu2017-1.1.0-ic19.0u5

(Continued on next page)
**Platform Notes (Continued)**

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From /sys/devices/virtual/dmi/id

- BIOS: Lenovo -[TEE151L-2.51]- 01/13/2020
- Vendor: Lenovo
- Product: ThinkSystem SR570 -[7Y02RCZ000]-
- Product Family: ThinkSystem
- Serial: 1234567890

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- Memory:
  - 4x NO DIMM NO DIMM
  - 12x SK Hynix HMA82GR7CJR8N-WM 16 GB 2 rank 2933

(End of data from sysinfo program)

**Compiler Version Notes**

```
C          | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------|------------------------------------------------------
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.5.281 Build 20190815 |
Copyright (C) 1985–2019 Intel Corporation. All rights reserved.

C++        | 508.namd_r(base) 510.parest_r(base)
------------|------------------------------------------------------
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.5.281 Build 20190815 |
Copyright (C) 1985–2019 Intel Corporation. All rights reserved.

C++, C     | 511.povray_r(base) 526.blender_r(base)
------------|------------------------------------------------------
| Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.5.281 Build 20190815 |
Copyright (C) 1985–2019 Intel Corporation. All rights reserved.
| Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.5.281 Build 20190815 |
```

(Continued on next page)
**Compiler Version Notes (Continued)**

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
==============================================================================
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.5.281 Build 20190815
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==============================================================================
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
==============================================================================
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  64, Version 19.0.5.281 Build 20190815
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.5.281 Build 20190815
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

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**Base Compiler Invocation**

C benchmarks:
  icc

C++ benchmarks:
  icpc

Fortran benchmarks:
  ifort
Lenovo Global Technology
ThinkSystem SR570
(2.10 GHz, Intel Xeon Gold 5218R)

SPECrete\textsuperscript{®}2017\_fp\_base = 190
SPECrete\textsuperscript{®}2017\_fp\_peak = Not Run

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<td>Software Availability:</td>
<td>Sep-2019</td>
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**Base Compiler Invocation (Continued)**

Benchmarks using both Fortran and C:
ifort icc

Benchmarks using both C and C++:
icpc icc

Benchmarks using Fortran, C, and C++:
icpc icc ifort

**Base Portability Flags**

503.bwaves\_r -DSPEC\_LP64
507.cactuBSSN\_r -DSPEC\_LP64
508.namd\_r -DSPEC\_LP64
510.parest\_r -DSPEC\_LP64
511.povray\_r -DSPEC\_LP64
519.lbm\_r -DSPEC\_LP64
521.wrf\_r -DSPEC\_LP64 -DSPEC\_CASE\_FLAG -convert big_endian
526.blender\_r -DSPEC\_LP64 -DSPEC\_Linux -funsigned\_char
527.cam4\_r -DSPEC\_LP64 -DSPEC\_CASE\_FLAG
538.imagick\_r -DSPEC\_LP64
544.nab\_r -DSPEC\_LP64
549.fotonik3d\_r -DSPEC\_LP64
554.roms\_r -DSPEC\_LP64

**Base Optimization Flags**

C benchmarks:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-m64 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-m64 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

(Continued on next page)
Lenovo Global Technology
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SPECrate®2017_fp_base = 190
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Test Date: Mar-2020
Tested by: Lenovo Global Technology
Hardware Availability: Mar-2020
Software Availability: Sep-2019

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

Benchmarks using both C and C++:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-m64 -std=c11 -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-F.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-F.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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