# SPEC CPU®2017 Floating Point Rate Result

## NEC Corporation

Express5800/R120h-1M (Intel Xeon Silver 4210)

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Mar-2020</th>
</tr>
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<tbody>
<tr>
<td>CPU2017 License:</td>
<td>9006</td>
</tr>
<tr>
<td>Test Sponsor:</td>
<td>NEC Corporation</td>
</tr>
<tr>
<td>Tested by:</td>
<td>NEC Corporation</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Dec-2019</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Sep-2019</td>
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<table>
<thead>
<tr>
<th>Software</th>
<th>SPECrate®2017_fp_base = 59.9</th>
<th>SPECrate®2017_fp_peak = 62.6</th>
</tr>
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<tbody>
<tr>
<td>OS:</td>
<td>Red Hat Enterprise Linux Server release 7.7 (Maipo)</td>
<td></td>
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<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux</td>
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<td>Parallel:</td>
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<td>File System:</td>
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<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
<td></td>
</tr>
<tr>
<td>Base Pointers:</td>
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<td></td>
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<tr>
<td>Peak Pointers:</td>
<td>64-bit</td>
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<tr>
<td>Power Management:</td>
<td>BIOS set to prefer performance at the cost of additional power usage</td>
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## Hardware

<table>
<thead>
<tr>
<th>503.bwaves_r</th>
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<tbody>
<tr>
<td>507.cactuBSSN_r</td>
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<tr>
<td>508.namd_r</td>
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<tr>
<td>510.parest_r</td>
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<td>519.lbm_r</td>
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<td>521.wrf_r</td>
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<td>544.nab_r</td>
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<tr>
<th>Copies</th>
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<th>SPECrate®2017_fp_peak (62.6)</th>
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</table>

**CPU Name:** Intel Xeon Silver 4210  
**Max MHz:** 3200  
**Nominal:** 2200  
**Enabled:** 10 cores, 1 chip, 2 threads/core  
**Orderable:** 1.2 chips  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 13.75 MB I+D on chip per chip  
**Other:** None  
**Memory:** 192 GB (12 x 16 GB 2Rx8 PC4-2933Y-R, running at 2400)  
**Storage:** 1 x 1 TB SATA, 7200 RPM, RAID 0  
**Other:** None
SPEC CPU®2017 Floating Point Rate Result

NEC Corporation

Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrate®2017_fp_base = 59.9
SPECrate®2017_fp_peak = 62.6

Results Table

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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The taskset mechanism was used to bind copies to processors. The config file option 'submit' was used to generate taskset commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

sync; echo 3 > /proc/sys/vm/drop_caches

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result
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NEC Corporation
Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrate®2017_fp_base = 59.9
SPECrate®2017_fp_peak = 62.6

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Test Date: Mar-2020
Tested by: NEC Corporation
Hardware Availability: Dec-2019
Software Availability: Sep-2019

General Notes (Continued)
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Thermal Configuration: Maximum Cooling
Workload Profile: General Throughput Compute
Memory Patrol Scrubbing: Disabled
LLC Dead Line Allocation: Disabled
LLC Prefetch: Enabled
Enhanced Processor Performance: Enabled
Workload Profile: Custom
Advanced Memory Protection: Advanced ECC Support
Sub-NUMA Clustering: Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edeb1e6e46a485a0011
running on r120h1m Mon Mar 23 09:30:04 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
 1 "physical id"s (chips)
 20 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 20
On-line CPU(s) list: 0-19
Thread(s) per core: 2

(Continued on next page)
**SPEC CPU®2017 Floating Point Rate Result**
Copyright 2017-2020 Standard Performance Evaluation Corporation

**NEC Corporation**

**Express5800/R120h-1M (Intel Xeon Silver 4210)**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
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<td>9006</td>
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</tr>
</tbody>
</table>

### SPECrate®2017_fp_base = 59.9
### SPECrate®2017_fp_peak = 62.6

**Platform Notes (Continued)**

- **Core(s) per socket:** 10
- **Socket(s):** 1
- **NUMA node(s):** 1
- **Vendor ID:** GenuineIntel
- **CPU family:** 6
- **Model:** 85
- **Model name:** Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
- **Stepping:** 6
- **CPU MHz:** 2200.000
- **BogoMIPS:** 4400.00
- **Virtualization:** VT-x
- **L1d cache:** 32K
- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 14080K
- **NUMA node0 CPU(s):** 0-19
- **Flags:** fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl apic cpuid nonstop_tsc aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer tsc搅 handwriting syscall elfi msr x save avx f16c rdrand lahf_lm abm 3nowprefetch epb cat l3 invpcid_single intel_ppln intel_pt ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bm11 hle avx2 smep bmi2 erms invpcid rtm cqm mpix rdt_a avx512f avx512dq rdseed adx clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsave xstate zpt avx f16c rdrand lahf_lm abm 3nowprefetch epb cat l3 invpcid_single intel_ppln intel_pt ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bm11 hle avx2 smep bmi2 erms invpcid rtm cqm mpix rdt_a avx512f avx512dq rdseed adx clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsave xstate zpt avx f16c rdrand lahf_lm abm 3nowprefetch epb cat l3 invpcid_single intel_ppln intel_pt ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bm11 hle avx2 smep bmi2 erms invpcid rtm cqm mpix rdt_a avx512f avx512dq rdseed adx clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsave xstate zpt avx f16c rdrand lahf_lm abm 3nowprefetch epb cat l3 invpcid_single intel_ppln intel_pt ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bm11 hle avx2 smep bmi2 erms invpcid rtm cqm mpix rdt_a avx512f avx512dq rdseed adx clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsave xstate zpt avx f16c rdrand lahf_lm abm 3nowprefetch epb cat l3 invpcid_single intel_ppln intel_pt ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bm11 hle avx2 smep bmi2 erms invpcid rtm cqm mpix rdt_a avx512f avx512dq rdseed adx clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsave xstate zpt avx f16c rdrand lahf_lm abm 3nowprefetch epb cat l3 invpcid_single intel_ppln intel_pt ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bm11 hle avx2 smep bmi2 erms invpcid rtm cqm mpix rdt_a avx512f avx512dq rdseed adx clflushopt clwb avx512cd avx512bw avx512vl xsaveopt xsave xstate zpt avx f16c rdrand lahf_lm abm 3nowprefetch epb cat l3 invpcid_single intel_ppln intel_pt ssbd mba ibrs ibpb stibp ibrs enhanced tpr_shadow vnni flexpriority ept vpid fsgsbase tsc_adjust bm11 hle avx2 smep bmi2 erms invpcid rtm cqm mpix rdt_a avx512f avx512dq rdseed adxlabel flush_l1d arch_capabilities

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 1 nodes (0)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
node 0 size: 196265 MB
node 0 free: 191425 MB
node distances:
node 0
  0: 10

From /proc/meminfo

MemTotal: 197745944 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

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CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Mar-2020
Hardware Availability: Dec-2019
Software Availability: Sep-2019

Platform Notes (Continued)

From /etc/*release* /etc/*version*
  os-release:
    NAME="Red Hat Enterprise Linux Server"
    VERSION="7.7 (Maipo)"
    ID="rhel"
    ID_LIKE="fedora"
    VARIANT="Server"
    VARIANT_ID="server"
    VERSION_ID="7.7"
    PRETTY_NAME="Red Hat Enterprise Linux Server 7.7 (Maipo)"
  redhat-release: Red Hat Enterprise Linux Server release 7.7 (Maipo)
  system-release: Red Hat Enterprise Linux Server release 7.7 (Maipo)
  system-release-cpe: cpe:/o:redhat:enterprise_linux:7.7:ga:server

uname -a:
  Linux r120h1m 3.10.0-1062.1.1.el7.x86_64 #1 SMP Tue Aug 13 18:39:59 UTC 2019 x86_64
  x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: Load fences, usercopy/swapgs barriers and __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Full retpoline, IBPB

run-level 3 Mar 23 09:24

SPEC is set to: /home/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda3  ext4  908G  45G  817G  6% /

From /sys/devices/virtual/dmi/id
  BIOS: NEC U32 11/13/2019
  Vendor: NEC
  Product: Express5800/R120h-1M
  Serial: JPN0084094

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is 'intended to allow hardware to be accurately determined', but the intent may not be met, as there are frequent changes to hardware, firmware, and the 'DMTF SMBIOS' standard.
Memory:
  12x HPE P03050-091 16 GB 2 rank 2933

(Continued on next page)
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NEC Corporation

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CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Mar-2020
Hardware Availability: Dec-2019
Software Availability: Sep-2019

Platform Notes (Continued)

12x UNKNOWN NOT AVAILABLE

(End of data from sysinfo program)
Regarding the sysinfo display about the memory speed, the correct configured
memory speed is 2400 MT/s. The dmidecode description should be as follows:
12x HPE P03050-091 16 GB 2 rank 2933, configured at 2400

Compiler Version Notes

==============================================================================
| C               | 519.lbm_r(base, peak) 538.imagick_r(base, peak)
|                 | 544.nab_r(base, peak)  |
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
| C++             | 508.namd_r(base, peak) 510.parest_r(base, peak) |
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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==============================================================================
| C++, C          | 511.povray_r(base, peak) 526.blender_r(base, peak) |
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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------------------------------------------------------------------------------

==============================================================================
| C++, C, Fortran | 507.cactusBSSN_r(base, peak) |
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
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(Continued on next page)
NEC Corporation

Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrater®2017_fp_base = 59.9
SPECrater®2017_fp_peak = 62.6

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Mar-2020
Hardware Availability: Dec-2019
Software Availability: Sep-2019

Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
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Fortran

| 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base, peak) |

==============================================================================

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
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==============================================================================

Fortran, C

| 521.wrf_r(base, peak) 527.cam4_r(base, peak) |

==============================================================================

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64, Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64
SPEC CPU®2017 Floating Point Rate Result

NEC Corporation

Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrate®2017_fp_base = 59.9
SPECrate®2017_fp_peak = 62.6

CPU2017 License: 9006
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Test Date: Mar-2020
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Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte
Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.lbm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: basepeak = yes

C++ benchmarks:
508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4
SPEC CPU®2017 Floating Point Rate Result

NEC Corporation

Express5800/R120h-1M (Intel Xeon Silver 4210)

SPECrate®2017_fp_base = 59.9
SPECrate®2017_fp_peak = 62.6

CPU2017 License: 9006
Test Sponsor: NEC Corporation
Tested by: NEC Corporation

Test Date: Mar-2020
Hardware Availability: Dec-2019
Software Availability: Sep-2019

Peak Optimization Flags (Continued)

510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:

521.wrf_r: basepeak = yes

527.cam4_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: basepeak = yes

Benchmarks using Fortran, C, and C++:

-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

The flags files that were used to format this result can be browsed at

http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-R120h-RevE.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/NEC-Platform-Settings-V1.2-R120h-RevE.xml
### SPEC CPU®2017 Floating Point Rate Result

#### NEC Corporation

**Express5800/R120h-1M (Intel Xeon Silver 4210)**

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<thead>
<tr>
<th>SPECrate®2017_fp_base = 59.9</th>
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**CPU2017 License:** 9006  
**Test Sponsor:** NEC Corporation  
**Tested by:** NEC Corporation  

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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