## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**
Cisco UCS B200 M5 (Intel Xeon Silver 4210R, 2.40GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>101</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Mar-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

### Hardware

- **CPU Name:** Intel Xeon Silver 4210R  
- **Max MHz:** 3200  
- **Nominal:** 2400  
- **Enabled:** 20 cores, 2 chips, 2 threads/core  
- **Orderable:** 1,2 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 13.75 MB I+D on chip per chip  
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)  
- **Storage:** 1 x 240 GB SSD SATA

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
  4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** No  
- **Firmware:** Version 4.0.4b released Apr-2019  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable

**Power Management:** BIOS set to prefer performance at the cost of additional power usage

---

**Copies**

<table>
<thead>
<tr>
<th>Benchmark</th>
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<th>SPECrate®2017_fp_base</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>40</td>
<td>86.7</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>40</td>
<td>87.3</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>40</td>
<td>52.6</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>40</td>
<td>51.9</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>40</td>
<td>135</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>40</td>
<td>51.9</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>40</td>
<td>98.3</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>40</td>
<td>110</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>40</td>
<td>120</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>40</td>
<td>252</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>40</td>
<td>184</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>40</td>
<td>69.4</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>40</td>
<td>42.6</td>
</tr>
</tbody>
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**Averages:**

- **SPECrate®2017_fp_base (101)**
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</tr>
</tbody>
</table>

**SPECrate®2017_fp_base** = 101  
**SPECrate®2017_fp_peak** = Not Run

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### Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>40</td>
<td>1809</td>
<td>222</td>
<td>1809</td>
<td>222</td>
<td>1810</td>
<td>222</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>40</td>
<td>584</td>
<td>86.7</td>
<td>585</td>
<td>86.6</td>
<td>584</td>
<td>86.8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>508.namd_r</td>
<td>40</td>
<td>436</td>
<td>87.2</td>
<td>435</td>
<td>87.3</td>
<td>435</td>
<td>87.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>510.parest_r</td>
<td>40</td>
<td>1975</td>
<td>53.0</td>
<td>1995</td>
<td>52.4</td>
<td>1991</td>
<td>52.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>511.povray_r</td>
<td>40</td>
<td>687</td>
<td>136</td>
<td>696</td>
<td>134</td>
<td>691</td>
<td>135</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>40</td>
<td>813</td>
<td>51.9</td>
<td>812</td>
<td>51.9</td>
<td>813</td>
<td>51.9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>40</td>
<td>908</td>
<td>98.6</td>
<td>912</td>
<td>98.3</td>
<td>932</td>
<td>96.2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td>40</td>
<td>553</td>
<td>110</td>
<td>555</td>
<td>110</td>
<td>554</td>
<td>110</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td>40</td>
<td>584</td>
<td>120</td>
<td>583</td>
<td>120</td>
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<td>120</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>40</td>
<td>392</td>
<td>254</td>
<td>396</td>
<td>251</td>
<td>395</td>
<td>252</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td>40</td>
<td>365</td>
<td>184</td>
<td>368</td>
<td>183</td>
<td>360</td>
<td>187</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>40</td>
<td>2246</td>
<td>69.4</td>
<td>2245</td>
<td>69.4</td>
<td>2245</td>
<td>69.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>554.roms_r</td>
<td>40</td>
<td>1492</td>
<td>42.6</td>
<td>1493</td>
<td>42.6</td>
<td>1493</td>
<td>42.6</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

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### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3> /proc/sys/vm/drop_caches
```
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Silver 4210R, 2.40GHz)

SPECrater®2017_fp_base = 101
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

runCPU command invoked through numactl i.e.:
numactl --interleave=all runCPU <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbb1e6e46a485a0011
running on linux-1t71 Sat Mar 14 22:17:36 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name: Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 10
siblings: 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2

(Continued on next page)
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Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4210R CPU @ 2.40GHz
Stepping: 7
CPU MHz: 2400.000
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9,20-29
NUMA node1 CPU(s): 10-19,30-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtsscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcd cca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat _13 cpdp_l3 invpcid_single intel_pinn mba tpr_shadow vmxlimit flexpriority ept
vpd fsgsbase tsc_adjust bni hle avx2 smep bmi2 emms invpcid rtm cmqm mxr rdt_a
avx512f avx512dq rsseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves ecxgetbv1 xsavec cqm_llc cqm_occu llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat slat pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From /proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
  node 0 size: 386372 MB
  node 0 free: 379377 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
  node 1 size: 387044 MB
  node 1 free: 381414 MB
  node distances:
    node 0: 10 21
    node 1: 21 10

(Continued on next page)
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| SPECrate®2017_fp_base = 101 |
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CPU2017 License: 9019
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Platform Notes (Continued)

MemTotal: 791979260 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-1t71 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Mar 14 17:25

SPEC is set to: /home/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sdb1 btrfs 224G 17G 207G 8% /home

From /sys/devices/virtual/dmi/id
  BIOS: Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
  Vendor: Cisco Systems Inc
  Product: UCSB-B200-M5
  Serial: FCH221572HW

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:

(Continued on next page)
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Test Date: Mar-2020
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Platform Notes (Continued)

24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400
(End of data from sysinfo program)

Compiler Version Notes

<table>
<thead>
<tr>
<th>Language</th>
<th>Programs</th>
</tr>
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<tbody>
<tr>
<td>C</td>
<td>519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)</td>
</tr>
<tr>
<td></td>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
</tr>
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<td></td>
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</tbody>
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<td></td>
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</tr>
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<td></td>
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<tr>
<td></td>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
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Compiler Version Notes (Continued)

==============================================================================
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Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64

(Continued on next page)
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### Base Portability Flags (Continued)

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- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

**C++ benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

**Fortran benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

**Benchmarks using both Fortran and C:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

**Benchmarks using both C and C++:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

**Benchmarks using Fortran, C, and C++:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte
## Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Silver 4210R, 2.40GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>101</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date</td>
<td>Mar-2020</td>
</tr>
<tr>
<td>Hardware Availability</td>
<td>Feb-2020</td>
</tr>
<tr>
<td>Software Availability</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


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