### Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5218R, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>204</td>
</tr>
</tbody>
</table>

#### CPU2017 License:
9019

**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Mar-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
<th>SPECrate®2017_fp_peak</th>
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<tbody>
<tr>
<td>503.bwaves_r 80</td>
<td>161</td>
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</tr>
<tr>
<td>507.cactuBSSN_r 80</td>
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<td>508.namd_r 80</td>
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<td>510.parest_r 80</td>
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<td>511.povray_r 80</td>
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<tr>
<td>519.lbm_r 80</td>
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<td>521.wrf_r 80</td>
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<tr>
<td>526.blender_r 80</td>
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<td>527.cam4_r 80</td>
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<td>538.imagick_r 80</td>
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<td>544.nab_r 80</td>
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<tr>
<td>549.fotonik3d_r 80</td>
<td>152</td>
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</tr>
<tr>
<td>554.roms_r 80</td>
<td>90.7</td>
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---

#### Hardware

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon Gold 5218R</th>
</tr>
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<tbody>
<tr>
<td>Max MHz:</td>
<td>4000</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2100</td>
</tr>
<tr>
<td>Enabled:</td>
<td>40 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1,2 Chips</td>
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<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
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<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
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<td>L3:</td>
<td>27.5 MB I+D on chip per chip</td>
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<td>Other:</td>
<td>None</td>
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<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)</td>
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<tr>
<td>Storage:</td>
<td>1 x 240 GB SSD SATA</td>
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<td>Other:</td>
<td>None</td>
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#### Software

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</th>
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</thead>
<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
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<tr>
<td>Parallel:</td>
<td>No</td>
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<tr>
<td>Firmware:</td>
<td>Version 4.0.4b released Apr-2019 btrfs</td>
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<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
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<tr>
<td>Base Pointers:</td>
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<td>Peak Pointers:</td>
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<td>Other:</td>
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<td>Power Management:</td>
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## Results Table

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</table>

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**Submit Notes**

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

**Operating System Notes**

Stack size set to unlimited using "ulimit -s unlimited"

**Environment Variables Notes**

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

**General Notes**

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
```

(Continued on next page)
SPEC CPU®2017 Floating Point Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5218R, 2.10GHz)

SPECrat®2017_fp_base = 200
SPECrat®2017_fp_peak = 204

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7ed1be6e46a485a0011
running on linux-bo6o Sat Mar 14 23:11:49 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz
  2 "physical id"s (chips)
  80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 40
physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 2
Core(s) per socket: 20
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel

(Continued on next page)
## Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Platform Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU family:</td>
</tr>
<tr>
<td>Model:</td>
</tr>
<tr>
<td>Model name: Intel(R) Xeon(R) Gold 5218R CPU @ 2.10GHz</td>
</tr>
<tr>
<td>Stepping:</td>
</tr>
<tr>
<td>CPU MHz:</td>
</tr>
<tr>
<td>CPU max MHz:</td>
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<tr>
<td>CPU min MHz:</td>
</tr>
<tr>
<td>BogoMIPS:</td>
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<tr>
<td>Virtualization: VT-x</td>
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<td>L1i cache:</td>
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<td>L2 cache:</td>
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<td>L3 cache:</td>
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<td>NUMA node0 CPU(s):</td>
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<td>NUMA node1 CPU(s):</td>
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<td>NUMA node2 CPU(s):</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
</tr>
<tr>
<td>Flags:</td>
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</tbody>
</table>

```
/fproc/cpuinfo
/cache data
cache size : 28160 KB
```

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

```
available: 4 nodes (0-3)
nod 0 cpus: 0 1 2 3 6 10 11 12 15 16 40 41 42 45 46 50 51 52 55 56
node 0 size: 192090 MB
node 0 free: 179940 MB
node 1 cpus: 3 4 7 8 9 13 14 17 18 19 43 44 47 48 49 53 54 57 28 59
node 1 size: 193521 MB
node 1 free: 184788 MB
node 2 cpus: 20 21 22 25 26 30 31 32 35 36 60 61 62 65 66 70 71 72 75 76
node 2 size: 193521 MB
node 2 free: 185162 MB
node 3 cpus: 23 24 27 28 29 33 34 37 38 39 63 64 67 68 69 73 74 77 78 79
node 3 size: 193490 MB
```

(Continued on next page)
Platform Notes (Continued)

node 3 free: 185084 MB
node distances:
node 0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791167672 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-bo6o 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Mar 14 13:25

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb1 btrfs 224G 41G 183G 19% /home

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5218R, 2.10GHz)

SPECrate\textsuperscript{\textregistered}2017\textsubscript{fp}_base = 200
SPECrate\textsuperscript{\textregistered}2017\textsubscript{fp}_peak = 204

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Mar-2020
Hardware Availability: Feb-2020
Tested by: Cisco Systems
Software Availability: May-2019

Platform Notes (Continued)

Vendor: Cisco Systems Inc
Product: UCSB-B200-M5
Serial: FCH21437LAT

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

C
519.libm_r(base, peak) 538.imagick_r(base, peak)
544.nab_r(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
508.namd_r(base, peak) 510.parest_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C
511.povray_r(base, peak) 526.blender_r(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++, C, Fortran
507.cactuBSSN_r(base, peak)

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5218R, 2.10GHz)

SPECrater®2017_fp_base = 200
SPECrater®2017_fp_peak = 204

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5218R, 2.10GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 200
SPECrate®2017_fp_peak = 204

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Base Compiler Invocation (Continued)

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5218R, 2.10GHz)

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<th>SPECrate®2017_fp_peak = 204</th>
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<td>Test Date: Mar-2020</td>
</tr>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Feb-2020</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

### Base Optimization Flags (Continued)

Benchmarks using both C and C++:
- `-xCORE-AVX512` `-ipo` `-O3` `-no-prec-div` `-gopt-prefetch`
  `-ffinite-math-only` `-gopt-mem-layout-trans=4`

Benchmarks using Fortran, C, and C++:
- `-xCORE-AVX512` `-ipo` `-O3` `-no-prec-div` `-gopt-prefetch`
  `-ffinite-math-only` `-gopt-mem-layout-trans=4` `-auto`
  `-nostandard-realloc-lhs` `-align array32byte`

### Peak Compiler Invocation

C benchmarks:
- `icc -m64 -std=c11`

C++ benchmarks:
- `icpc -m64`

Fortran benchmarks:
- `ifort -m64`

Benchmarks using both Fortran and C:
- `ifort -m64 icc -m64 -std=c11`

Benchmarks using both C and C++:
- `icpc -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
- `icpc -m64 icc -m64 -std=c11 ifort -m64`

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

C benchmarks:
- `519.lbm_r -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512`
  `-O3` `-no-prec-div` `-gopt-prefetch` `-ffinite-math-only`
  `-gopt-mem-layout-trans=4`

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 5218R, 2.10GHz)

SPEC CPU®2017 Floating Point Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_fp_base = 200
SPECrate®2017_fp_peak = 204

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CPU2017 License: 9019
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Peak Optimization Flags (Continued)

538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512
-O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch

(Continued on next page)
## Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++ (continued):

-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links: