Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

SPECrater2017_int_base = 54.4
SPECrater2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Hardware

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<tr>
<td>502.gcc_r 16</td>
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<tr>
<td>520.omnetpp_r 16</td>
<td>38.9</td>
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<tr>
<td>523.xalancbk_r 16</td>
<td>65.4</td>
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<tr>
<td>525.x264_r 16</td>
<td>109</td>
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<tr>
<td>531.deepsjeng_r 16</td>
<td>43.3</td>
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<tr>
<td>541.leea_r 16</td>
<td>36.0</td>
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<tr>
<td>548.exchange2_r 16</td>
<td>114</td>
</tr>
<tr>
<td>557.xz_r 16</td>
<td>31.2</td>
</tr>
</tbody>
</table>

Software

OS: SUSE Linux Enterprise Server 15 (x86_64)
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: No
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: BIOS set to prefer performance at the cost of additional power usage

CPU Name: Intel Xeon Bronze 3206R
Max MHz: 1900
Nominal: 1900
Enabled: 16 cores, 2 chips
Orderable: 1,2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 11 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2133)
Storage: 1 x 240 GB SSD SATA
Other: None
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

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SPECrate®2017_int_base = 54.4
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Results Table

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</tbody>
</table>

SPECrate®2017_int_base = 54.4
SPECrate®2017_int_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes
The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor.
For details, please see the config file.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = 
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R,
1.90GHz)

General Notes (Continued)

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbl6e46a485a0011
running on linux-us1o Sat Mar 14 17:44:33 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
  2 "physical id"s (chips)
  16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_int_base = 54.4
SPECrate®2017_int_peak = Not Run

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

Model: 85
Model name: Intel(R) Xeon(R) Bronze 3206R CPU @ 1.90GHz
Stepping: 7
CPU MHz: 1900.000
CPU max MHz: 1900.0000
CPU min MHz: 1000.0000
BogoMIPS: 3800.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 11264K
NUMA node0 CPU(s): 0-7
NUMA node1 CPU(s): 8-15

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmonperf tsc_known_freq pni pclmulqdq dtses64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 cdp_l3 invpcid_single intel_pmmu mca cpuacct cpuid

From /proc/cpuinfo cache data
  cache size: 11264 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7
node 0 size: 386374 MB
node 0 free: 385390 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 387047 MB
node 1 free: 386520 MB
node distances:
node 0 1
  0: 10 21
  1: 21 10

From /proc/meminfo
MemTotal: 791984136 kB
hugePages_Total: 0

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

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</tbody>
</table>

**Platform Notes (Continued)**

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

```
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"
```

uname -a:
```
Linux linux-us1o 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- CVE-2018-3620 (L1 Terminal Fault): No status reported
- Microarchitectural Data Sampling: No status reported
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Mar 14 17:29

SPEC is set to: /home/cpu2017
```
Filesystem  Type  Size  Used Avail Use% Mounted on
/dev/sdb2    btrfs  224G  6.4G  217G   3% /home
```

From /sys/devices/virtual/dmi/id
```
BIOS:    Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
Vendor:  Cisco Systems Inc
Product: UCSB-B200-M5
Serial:  FCH22137XAV
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
```
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2133
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)  

SPECratenumber_int_base = 54.4
SPECratenumber_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Mar-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

(End of data from sysinfo program)

Compiler Version Notes

------------------------------------------------------------------------------
| C       | 500.perlbench_r(base) 502.gcc_r(base) 505.mcf_r(base) 525.x264_r(base) 557.xz_r(base) |
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
| C++     | 520.omnetpp_r(base) 523.xalancbmk_r(base) 531.deepsjeng_r(base) 541.leela_r(base) |
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

------------------------------------------------------------------------------
| Fortran | 548.exchange2_r(base) |
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64
SPEC CPU®2017 Integer Rate Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Bronze 3206R, 1.90GHz)

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Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.keela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-1qkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
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