Dell Inc.

PowerEdge T440 (Intel Xeon Silver 4216, 2.10 GHz)

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Mar-2020
Hardware Availability: Dec-2019
Software Availability: Jun-2019

SPECrater®2017_fp_base = 162
SPECrater®2017_fp_peak = 167

<table>
<thead>
<tr>
<th>Spec Test</th>
<th>Benchmark Name</th>
<th>Copies</th>
<th>SPECrate®2017_fp_base</th>
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<tr>
<td>554.roms_r</td>
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<td>380</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Hardware

CPU Name: Intel Xeon Silver 4216
Max MHz: 3200
Nominal: 2100
Enabled: 32 cores, 2 chips, 2 threads/core
Orderable: 1,2 chip
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per core
Other: None
Memory: 384 GB (12 x 32 GB 2Rx8 PC4-2666V-R)
Storage: 1 x 960 GB SATA SSD
Other: None

Software

OS: Suse Linux Enterprise Server 15 SP1
kernel 4.12.14-195-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux
Parallel: No
Firmware: Version 2.5.4 released Jan-2020
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: BIOS set to prefer performance at the cost of additional power usage.
## Dell Inc.

**PowerEdge T440 (Intel Xeon Silver 4216, 2.10 GHz)**

**SPECrates**:
- **SPECrates\textsuperscript{2017} \_fp\_base = 162**
- **SPECrates\textsuperscript{2017} \_fp\_peak = 167**

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### Results Table

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**SPECrates\textsuperscript{2017} \_fp\_base = 162**

**SPECrates\textsuperscript{2017} \_fp\_peak = 167**

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

LD\_LIBRARY\_PATH = ":/home/cpu2017/lib/intel64"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Dell Inc.

PowerEdge T440 (Intel Xeon Silver 4216, 2.10 GHz)

**SPEC CPU®2017 Floating Point Rate Result**

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**CPU2017 License:** 55  
**Test Sponsor:** Dell Inc.  
**Tested by:** Dell Inc.  
**Test Date:** Mar-2020  
**Hardware Availability:** Dec-2019  
**Software Availability:** Jun-2019

**General Notes (Continued)**

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

runcpu command invoked through numactl i.e.:

```
numactl --interleave=all runcpu <etc>
```

**Platform Notes**

**BIOS settings:**
- Sub NUMA Cluster enabled
- Virtualization Technology disabled
- DCU Streamer Prefetcher disabled
- System Profile set to Custom
- CPU Performance set to Maximum Performance
- C States set to Autonomous
- C1E disabled
- Uncore Frequency set to Dynamic
- Energy Efficiency Policy set to Performance
- Memory Patrol Scrub disabled
- Logical Processor enabled
- CPU Interconnect Bus Link Power Management enabled
- PCI ASPM L1 Link Power Management enabled

**Sysinfo program**

```
/home/cpu2017/bin/sysinfo
```

Rev: r6365 of 2019-08-21 295195f888a3d7edbble6e46a485a0011

running on linux-g3ob Wed Mar 11 12:38:33 2020

**SUT (System Under Test) info as seen by some common utilities.**

For more information on this section, see

```
https://www.spec.org/cpu2017/Docs/config.html#sysinfo
```

From `/proc/cpuinfo`

```
model name : Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From `lscpu`:

```
(Continued on next page)
Dell Inc. PowerEdge T440 (Intel Xeon Silver 4216, 2.10 GHz)

Dell Inc.

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

SPECrate®2017_fp_base = 162
SPECrate®2017_fp_peak = 167

Platform Notes (Continued)

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4216 CPU @ 2.10GHz
Stepping: 6
CPU MHz: 2100.000
BogoMIPS: 4200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 22528K
NUMA node0 CPU(s): 0,2,4,6,8,10,12,14,16,18,20,22,24,26,28,30,32,34,36,38,40,42,44,46,48,50,52,54,56,58
NUMA node1 CPU(s): 1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16
x2apic pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave
avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3
invpcid_single intel_puin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnumi
flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm
cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd
avx512bw avx512vl xsavesopt xsaveopt xsave xstate qsaves qcm_llc qcm_occup_llc qcm_mbb_total
qcm_mbb_local dtherm ida arat pln pts pklu ospke avx512_vnni md_clear flush_l1d
arch_capabilities

/proc/cpuinfo cache data
cache size : 22528 KB
From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
documented chip:
available: 2 nodes (0-1)

(Continued on next page)
Dell Inc.

PowerEdge T440 (Intel Xeon Silver 4216, 2.10 GHz)

SPECCPU2017 Floating Point Rate Result

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SPECrate®2017_fp_base = 162
SPECrate®2017_fp_peak = 167

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Mar-2020
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Platform Notes (Continued)

node 0 cpus: 0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 58 60 62
node 0 size: 192071 MB
node 0 free: 190948 MB
node 1 cpus: 1 3 5 7 9 11 13 15 17 19 21 23 25 27 29 31 33 35 37 39 41 43 45 47 49 51 53 55 57 59 61 63
node 1 size: 193499 MB
node 1 free: 192793 MB
node distances:
node 0 1
 0: 10 21
 1: 21 10

From /proc/meminfo
MemTotal:       394825140 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release*/etc/*version*
os-release:
  NAME="SLES"
  VERSION="15-SP1"
  VERSION_ID="15.1"
  PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
Linux linux-g3ob 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019 (8fba516)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Mar 11 05:50 last=5

SPEC is set to: /home/cpu2017

(Continued on next page)
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PowerEdge T440 (Intel Xeon Silver 4216, 2.10 GHz)  

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CPU2017 License: 55  
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---

**Platform Notes (Continued)**

```
Filesystem  Type  Size  Used  Avail  Use%  Mounted on
/dev/sda2   xfs    440G  46G   395G  11%  /
```

From /sys/devices/virtual/dmi/id

- BIOS: Dell Inc. 2.5.4 01/14/2020
- Vendor: Dell Inc.
- Product: PowerEdge T440
- Product Family: PowerEdge
- Serial: FBLH613

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

```
Memory:
  4x 00AD00B300AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
  8x 00AD063200AD HMA84GR7CJR4N-WM 32 GB 2 rank 2933
  4x Not Specified Not Specified
```

(End of data from sysinfo program)

---

**Compiler Version Notes**

```
C
```

---

```
| 519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)
```

---

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

---

```
C++
```

---

```
| 508.namd_r(base, peak) 510.parest_r(base, peak)
```

---

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

---

```
C++, C
```

---

```
| 511.povray_r(base, peak) 526.blender_r(base, peak)
```

---

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

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Compiler Version Notes (Continued)

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Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------------------------
C++, C, Fortran | 507.cactuBSSN_r(base, peak)
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Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------------------------
Fortran         | 503.bwaves_r(base, peak) 549.fotonik3d_r(base, peak) 554.roms_r(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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Fortran, C      | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
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-----------------------------------------------------------------------------------------------
Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

(Continued on next page)
Base Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.llvm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only

(Continued on next page)
Dell Inc.  
PowerEdge T440 (Intel Xeon Silver 4216, 2.10 GHz)  

SPEC CPU®2017 Floating Point Rate Result  

Copyright 2017-2020 Standard Performance Evaluation Corporation  

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<td></td>
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</table>

**Base Optimization Flags (Continued)**

Fortran benchmarks (continued):
- `-qopt-mem-layout-trans=4`  
- `-auto`  
- `-nostandard-realloc-lhs`  
- `-align array32byte`

Benchmarks using both Fortran and C:
- `-xCORE-AVX2`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`  
- `-auto`  
- `-nostandard-realloc-lhs`  
- `-align array32byte`

Benchmarks using both C and C++:
- `-xCORE-AVX2`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`

Benchmarks using Fortran, C, and C++:
- `-xCORE-AVX2`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-prefetch`  
- `-ffinite-math-only`  
- `-qopt-mem-layout-trans=4`  
- `-auto`  
- `-nostandard-realloc-lhs`  
- `-align array32byte`

**Peak Compiler Invocation**

C benchmarks:
- `icc -m64 -std=c11`

C++ benchmarks:
- `icpc -m64`

Fortran benchmarks:
- `ifort -m64`

Benchmarks using both Fortran and C:
- `ifort -m64 icc -m64 -std=c11`

Benchmarks using both C and C++:
- `icpc -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
- `icpc -m64 icc -m64 -std=c11 ifort -m64`

**Peak Portability Flags**

Same as Base Portability Flags
Dell Inc.  
PowerEdge T440 (Intel Xeon Silver 4216, 2.10 GHz)  

SPEC CPU®2017 Floating Point Rate Result

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SPECrate®2017_fp_base = 162
SPECrate®2017_fp_peak = 167

CPU2017 License: 55
Test Sponsor: Dell Inc.
Tested by: Dell Inc.

Test Date: Mar-2020
Hardware Availability: Dec-2019
Software Availability: Jun-2019

Peak Optimization Flags

C benchmarks:

519.lmb_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:

503.bwaves_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:

-prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX2 -O3
-no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

(Continued on next page)
<table>
<thead>
<tr>
<th>Dell Inc.</th>
<th>SPECrate®2017_fp_peak = 167</th>
</tr>
</thead>
<tbody>
<tr>
<td>PowerEdge T440 (Intel Xeon Silver 4216, 2.10 GHz)</td>
<td>SPECrate®2017_fp_base = 162</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 55  
**Test Date:** Mar-2020  
**Test Sponsor:** Dell Inc.  
**Hardware Availability:** Dec-2019  
**Tested by:** Dell Inc.  
**Software Availability:** Jun-2019

**Peak Optimization Flags (Continued)**

```bash
526.blender_r: -xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch 
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only 
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte
```

The flags files that were used to format this result can be browsed at  

You can also download the XML flags sources by saving the following links:  

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Tested with SPEC CPU®2017 v1.1.0 on 2020-03-11 13:38:32-0400.  
Originally published on 2020-03-31.