Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220R, 2.20GHz)  
SPECrater®2017_int_base = 269  
SPECrater®2017_int_peak = 280

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Hardware Availability: Feb-2020  
Software Availability: May-2019

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<tr>
<td>520.omnetpp_r</td>
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<tr>
<td>523.xalancbmk_r</td>
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<td>525.x264_r</td>
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<td>557.xz_r</td>
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<table>
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<tr>
<th>Hardware</th>
<th>Software</th>
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<tr>
<td>CPU Name: Intel Xeon Gold 5220R</td>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64)</td>
</tr>
<tr>
<td>Max MHz: 4000</td>
<td>4.12.14-23-default</td>
</tr>
<tr>
<td>Nominal: 2200</td>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++</td>
</tr>
<tr>
<td>Enabled: 48 cores, 2 chips, 2 threads/core</td>
<td>Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
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<tr>
<td>Orderable: 1.2 Chips</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
<td>Firmware: Version 4.0.4i released Aug-2019</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
<td>File System: btrfs</td>
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<tr>
<td>L3: 35.75 MB I+D on chip per chip</td>
<td>System State: Run level 3 (multi-user)</td>
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<tr>
<td>Other: None</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)</td>
<td>Peak Pointers: 32/64-bit</td>
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<tr>
<td>Storage: 1 x 960 GB SSD SAS</td>
<td>Other: jemalloc memory allocator V5.0.1</td>
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<td>Other: None</td>
<td>Power Management: BIOS set to prefer performance at the cost of additional power usage</td>
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</table>
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220R, 2.20GHz)

SPEC CPU®2017 Integer Rate Result

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SPEC CPU®2017_INT_BASE = 269
SPEC CPU®2017_INT_PEAK = 280

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
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Results Table

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<td>179</td>
<td>579</td>
<td>179</td>
<td>579</td>
<td>179</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH =
"/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220R, 2.20GHz)  

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 269
SPECrate®2017_int_peak = 280

Cisco Systems

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

General Notes (Continued)

numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbe6e46a485a0011
running on linux-cud8 Fri Feb 7 10:17:20 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name : Intel(R) Xeon(R) Gold 5220R CPU @ 2.20GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

From lscpu:

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24

(Continued on next page)
**SPEC CPU®2017 Integer Rate Result**

**Cisco Systems**

Cisco UCS C220 M5 (Intel Xeon Gold 5220R, 2.20GHz)

**SPECrate®2017_int_base = 269**

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<tr>
<td>Software Availability:</td>
<td>May-2019</td>
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</tbody>
</table>

**Platform Notes (Continued)**

Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5220R CPU @ 2.20GHz
Stepping: 7
CPU MHz: 2200.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 4400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 36608K
NUMA node0 CPU(s): 0-3,7-9,13-15,19,20,48-51,55-57,61-63,67,68
NUMA node1 CPU(s): 4-6,10-12,16-18,21-23,52-54,58-60,64-66,69-71
NUMA node2 CPU(s): 24-27,31,32,36-38,42-44,72-75,79,80,84-86,90-92
NUMA node3 CPU(s): 28-30,33-35,39-41,45-47,76-78,81-83,87-89,93-95

Flags: 
  fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpes gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nop1 xtopology nonstop_tsc cpuid aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault ebz cat_t13 cdp_l3 invpcid_single intel_pinn tpr_shadow vmx f16ni flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ibrms invpcid rtm cmx mxp rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsave xgetbvl xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs stibp dtherm ida arat pklm ptn hws hwp_act_window hwp_epp hwp_pkgreq pku ospke avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

Available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 7 8 9 13 14 15 19 20 48 49 50 51 55 56 57 61 62 63 67 68
node 0 size: 192118 MB
node 0 free: 191715 MB
node 1 cpus: 4 5 6 10 11 12 16 17 18 21 22 23 52 53 54 58 59 60 64 65 66 69 70 71
node 1 size: 193526 MB
node 1 free: 193277 MB
node 2 cpus: 24 25 26 27 31 32 36 37 38 42 43 44 72 73 74 75 79 80 84 85 86 90 91 92
node 2 size: 193497 MB

(Continued on next page)
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Platform Notes (Continued)

node 2 free: 193132 MB
node 3 cpus: 28 29 30 33 34 35 39 40 41 45 46 47 76 77 78 81 82 83 87 88 89 93 94 95
node 3 size: 193523 MB
node 3 free: 193296 MB
node distances:
  node: 0 1 2 3
    0: 10 11 21 21
    1: 11 10 21 21
    2: 21 21 10 11
    3: 21 21 11 10

From /proc/meminfo
  MemTotal: 791209068 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-cud8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Feb 7 05:17

SPEC is set to: /home/cpu2017

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<th>Use%</th>
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<td>/dev/sda2</td>
<td>btrfs</td>
<td>224G</td>
<td>38G</td>
<td>185G</td>
<td>17%</td>
<td>/home</td>
</tr>
</tbody>
</table>

(Continued on next page)
Platform Notes (Continued)

From /sys/devices/virtual/dmi/id
  BIOS: Cisco Systems, Inc. C220M5.4.0.4i.0.0831191119 08/31/2019
  Vendor: Cisco Systems Inc
  Product: UCSC-C220-M5SX
  Serial: WZP22380CRE

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

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SPEC CPU®2017 Integer Rate Result
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Compiler Version Notes (Continued)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
| 523.xalancbmk_r(peak) |
------------------------------------------------------------------------------

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
| 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) |
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak) |
------------------------------------------------------------------------------

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
| 523.xalancbmk_r(peak) |
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Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
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------------------------------------------------------------------------------
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Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------

Fortran | 548.exchange2_r(base, peak)
------------------------------------------------------------------------------

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220R, 2.20GHz)

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CPU2017 License: 9019
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---

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

---

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

---

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc
### Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5220R, 2.20GHz)

<table>
<thead>
<tr>
<th><strong>CPU2017 License:</strong> 9019</th>
<th><strong>Test Date:</strong> Feb-2020</th>
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<td><strong>Software Availability:</strong> May-2019</td>
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#### SPEC CPU®2017 Integer Rate Result

| **SPECrate®2017_int_base** = 269 | **SPECrate®2017_int_peak** = 280 |

---

### Peak Compiler Invocation

C benchmarks (except as noted below):
```
icc -m64 -std=c11
```

C++ benchmarks (except as noted below):
```
icpc -m64
```

Fortran benchmarks:
```
ifort -m64
```

---

### Peak Portability Flags

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Portability Flags</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>-DSPEC_LP64 -DSPEC_LINUX_X64</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>-D_FILE_OFFSET_BITS=64</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>-DSPEC_LP64</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>-DSPEC_LP64</td>
</tr>
</tbody>
</table>

---

### Peak Optimization Flags

C benchmarks:
```
500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -fno-strict-overflow -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc
```

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(Continued on next page)
Cisco Systems
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Peak Optimization Flags (Continued)

505.mcf_r (continued):
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264_r -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz_r: Same as 505.mcf_r

C++ benchmarks:

520.omnetpp_r -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

523.xalancbmk_r -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leea_r: Same as 520.omnetpp_r

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml
# SPEC CPU®2017 Integer Rate Result

## Cisco Systems
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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