Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6242R, 3.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Specspeed\textsuperscript{®}2017\textsubscript{int\_base} = 10.8
Specspeed\textsuperscript{®}2017\textsubscript{int\_peak} = 11.0

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
<td>CPU Name: Intel Xeon Gold 6242R</td>
</tr>
<tr>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
<td>Max MHz: 4100</td>
</tr>
<tr>
<td>Firmware: Version 4.0.4i released Aug-2019</td>
<td>Nominal: 3100</td>
</tr>
<tr>
<td>System State: Run level 3 (multi-user)</td>
<td>Enabled: 40 cores, 2 chips</td>
</tr>
<tr>
<td>Base Pointers: 64-bit</td>
<td>Orderable: 1.2 Chips</td>
</tr>
<tr>
<td>Peak Pointers: 64-bit</td>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>Other: jemalloc memory allocator V5.0.1</td>
<td>L2: 1 MB I+D on chip per core</td>
</tr>
<tr>
<td>Power Management: BIOS set to prefer performance at the cost of additional power usage</td>
<td>L3: 35.75 MB I+D on chip per chip</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed\textsuperscript{®}2017\textsubscript{int_base} (10.8)</th>
<th>SPECspeed\textsuperscript{®}2017\textsubscript{int_peak} (11.0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>40</td>
<td>8.35</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>40</td>
<td>9.06</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>40</td>
<td>9.57</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>40</td>
<td>8.55</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>40</td>
<td>13.0</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>40</td>
<td>14.8</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>40</td>
<td>5.73</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>40</td>
<td>5.02</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>40</td>
<td>17.5</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>40</td>
<td>24.0</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6242R, 3.10GHz)

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SPEC CPU®2017 Integer Speed Result

SPECspeed®2017_int_base = 10.8
SPECspeed®2017_int_peak = 11.0

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>40</td>
<td>248</td>
<td>7.14</td>
<td>247</td>
<td>7.19</td>
<td>250</td>
<td>7.09</td>
<td>40</td>
<td>213</td>
<td>8.35</td>
<td>214</td>
<td>8.31</td>
<td>212</td>
<td>8.39</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>40</td>
<td>384</td>
<td>10.4</td>
<td>385</td>
<td>10.3</td>
<td>382</td>
<td>10.4</td>
<td>40</td>
<td>375</td>
<td>10.6</td>
<td>378</td>
<td>10.5</td>
<td>374</td>
<td>10.6</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>40</td>
<td>359</td>
<td>13.1</td>
<td>360</td>
<td>13.1</td>
<td>361</td>
<td>13.1</td>
<td>40</td>
<td>359</td>
<td>13.2</td>
<td>357</td>
<td>13.2</td>
<td>357</td>
<td>13.2</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>40</td>
<td>109</td>
<td>13.0</td>
<td>109</td>
<td>13.0</td>
<td>109</td>
<td>13.0</td>
<td>40</td>
<td>110</td>
<td>12.9</td>
<td>109</td>
<td>13.0</td>
<td>109</td>
<td>13.0</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>40</td>
<td>119</td>
<td>14.8</td>
<td>119</td>
<td>14.8</td>
<td>119</td>
<td>14.8</td>
<td>40</td>
<td>120</td>
<td>14.7</td>
<td>119</td>
<td>14.8</td>
<td>119</td>
<td>14.8</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>40</td>
<td>250</td>
<td>5.74</td>
<td>250</td>
<td>5.73</td>
<td>250</td>
<td>5.73</td>
<td>40</td>
<td>250</td>
<td>5.73</td>
<td>250</td>
<td>5.73</td>
<td>250</td>
<td>5.74</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>40</td>
<td>340</td>
<td>5.02</td>
<td>339</td>
<td>5.03</td>
<td>339</td>
<td>5.03</td>
<td>40</td>
<td>340</td>
<td>5.02</td>
<td>340</td>
<td>5.02</td>
<td>340</td>
<td>5.02</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>40</td>
<td>168</td>
<td>17.5</td>
<td>167</td>
<td>17.6</td>
<td>169</td>
<td>17.4</td>
<td>40</td>
<td>167</td>
<td>17.6</td>
<td>168</td>
<td>17.5</td>
<td>167</td>
<td>17.6</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>40</td>
<td>257</td>
<td>24.0</td>
<td>258</td>
<td>24.0</td>
<td>258</td>
<td>24.0</td>
<td>40</td>
<td>256</td>
<td>24.2</td>
<td>255</td>
<td>24.2</td>
<td>255</td>
<td>24.2</td>
</tr>
</tbody>
</table>

RESULTS APPEAR IN THE ORDER IN WHICH THEY WERE RUN. BOLD UNDERLINED TEXT INDICATES A MEDIAN MEASUREMENT.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5
Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eb1e6e46a485a0011
running on linux-cud8 Thu Feb 27 23:03:23 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz
  2 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 20
physical 0: cores 0 1 2 3 5 6 9 10 12 13 16 17 18 19 20 21 24 26 27 28 29
physical 1: cores 0 1 2 3 5 6 10 11 12 13 16 17 18 19 21 24 26 27 28 29

From lscpu:
Architecture:        x86_64
CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
CPU(s):              40
On-line CPU(s) list: 0-39
Thread(s) per core:  1
Core(s) per socket:  20
Socket(s):           2
NUMA node(s):        2
Vendor ID:           GenuineIntel
CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Gold 6242R CPU @ 3.10GHz
Stepping:            7
CPU MHz:             3100.000
CPU max MHz:         4100.0000
CPU min MHz:         1200.0000
BogoMIPS:            6200.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K

(Continued on next page)
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 SPECspeed®2017_int_base = 10.8
 SPECspeed®2017_int_peak = 11.0

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Feb-2020
Software Availability: May-2019

Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 36068K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
 tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_ppin mba tpr_shadow vmni flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xgetbv1 xsave vmm lucm_llc vmm_occup_llc vmm_mbm_total vmm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospek avx512_vnni arch_capabilities ssbd

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
node 0 size: 385633 MB
node 0 free: 384888 MB
node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
node 1 size: 387027 MB
node 1 free: 386712 MB
node distances:
node 0 1
 0: 10 21
 1: 21 10

From /proc/meminfo
MemTotal: 791205016 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"

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Platform Notes (Continued)

```
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-cud8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Feb 27 23:02

SPEC is set to: /home/cpu2017
  Filesystem    Type   Size  Used Avail Use% Mounted on
  /dev/sdc2      btrfs  224G   38G  185G  18% /home

From /sys/devices/virtual/dmi/id
  BIOS: Cisco Systems, Inc. C220M5.4.0.41.0.0831191119 08/31/2019
  Vendor: Cisco Systems Inc
  Product: UCSC-C220-M5SX
  Serial: WZP22380CRE

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  Memory: 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
```

(End of data from sysinfo program)

Compiler Version Notes

```
C | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak)
   | 625.x264_s(base, peak) 657.xz_s(base, peak)
```

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 6242R, 3.10GHz)

| SPECspeed®2017_int_base | 10.8 |
| SPECspeed®2017_int_peak | 11.0 |

### Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---

### Base Compiler Invocation

**C benchmarks:**
```bash
ingcc -m64 -std=c11
```

**C++ benchmarks:**
```bash
icc -m64
```

**Fortran benchmarks:**
```bash
ifort -m64
```

### Base Portability Flags

- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
- 602.gcc_s: -DSPEC_LP64
- 605.mcf_s: -DSPEC_LP64
- 620.omnetpp_s: -DSPEC_LP64
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
- 625.x264_s: -DSPEC_LP64
- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64

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## Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 6242R, 3.10GHz)

<table>
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<tr>
<th>SPECspeed®2017_int_base = 10.8</th>
<th>SPECspeed®2017_int_peak = 11.0</th>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Feb-2020  
**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

<table>
<thead>
<tr>
<th>Command</th>
<th>Flags/Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>C benchmarks:</td>
<td>-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP</td>
</tr>
<tr>
<td></td>
<td>-L/usr/local/je5.0.1-64/lib -ljemalloc</td>
</tr>
<tr>
<td>C++ benchmarks:</td>
<td>-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4</td>
</tr>
<tr>
<td></td>
<td>-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc</td>
</tr>
<tr>
<td>Fortran benchmarks:</td>
<td>-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -nostandard-realloc-lhs</td>
</tr>
</tbody>
</table>

## Base Portability Flags (Continued)

657.xz_s: -DSPEC_LP64

## Base Optimization Flags

### C benchmarks:
- `-Wl,-z,muldefs`  
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-qopenmp`  
- `-DSPEC_OPENMP`  
- `-L/usr/local/je5.0.1-64/lib`  
- `-ljemalloc`

### C++ benchmarks:
- `-Wl,-z,muldefs`  
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64`  
- `-lqkmalloc`

### Fortran benchmarks:
- `-xCORE-AVX512`  
- `-ipo`  
- `-O3`  
- `-no-prec-div`  
- `-qopt-mem-layout-trans=4`  
- `-nostandard-realloc-lhs`

## Peak Compiler Invocation

### C benchmarks:
- `icc`  
- `-m64`  
- `-std=c11`

### C++ benchmarks:
- `icpc`  
- `-m64`

### Fortran benchmarks:
- `ifort`  
- `-m64`

## Peak Portability Flags

Same as Base Portability Flags
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Tested by: Cisco Systems
Hardware Availability: Feb-2020
Software Availability: May-2019

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3 -no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP -fno-strict-overflow -L/usr/local/je5.0.1-64/lib -ljemalloc

602gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3 -no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP -ipo

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -gopenmp -DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -pro-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3 -no-prec-div -DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

623.xalancbm_k_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

631.deepsjeng_s: Same as 623.xalancbm_k_s

641.leela_s: Same as 623.xalancbm_k_s

Fortran benchmarks:

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4

(Continued on next page)
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| SPECspeed®2017_int_base = 10.8 |
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**Hardware Availability:** Feb-2020  
**Software Availability:** May-2019

---

## Peak Optimization Flags (Continued)

Fortran benchmarks (continued):  
- nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at:  

You can also download the XML flags sources by saving the following links:  
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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