## SPEC CPU®2017 Floating Point Speed Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(2.70 GHz, Intel Xeon Gold 6258R)

### SPECspeed®2017_fp_base = 155  
### SPECspeed®2017_fp_peak = 156

- **CPU2017 License:** 3  
- **Test Sponsor:** HPE  
- **Hardware Availability:** Feb-2020  
- **Test Date:** Jan-2020  
- **Software Availability:** Jun-2019

#### Hardware

**CPU Name:** Intel Xeon Gold 6258R  
**Max MHz:** 4000  
**Nominal:** 2700  
**Enabled:** 56 cores, 2 chips  
**Orderable:** 1, 2 chip(s)  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 38.5 MB I+D on chip per chip  
**Other:** None  
**Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R)  
**Storage:** 1 x 400 GB SATA SSD  
**Other:** None

#### Software

**OS:** SUSE Linux Enterprise Server 15 SP1 (x86_64)  
**Kernel:** 4.12.14-195-default  
**Compiler:**  
- C/C++: Version 19.0.4.227 of Intel C/C++ Compiler Build 20190416 for Linux;  
- Fortran: Version 19.0.4.227 of Intel Fortran Compiler Build 20190416 for Linux  
**Parallel:** Yes  
**Firmware:** HPE BIOS Version 142 2.30 (12/10/2019) released Feb-2020  
**File System:** xfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** 64-bit  
**Other:** None  
**Power Management:** BIOS set to prefer performance at the cost of additional power usage

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS: SUSE Linux Enterprise Server 15 SP1 (x86_64)</td>
<td>CPU Name: Intel Xeon Gold 6258R</td>
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<td>Kernel: 4.12.14-195-default</td>
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<td>Peak Pointers: 64-bit</td>
<td>Storage: 1 x 400 GB SATA SSD</td>
</tr>
<tr>
<td>Other: None</td>
<td>Other: None</td>
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</tbody>
</table>

#### SPECspeed

**603.bwaves_s**  
**607.cactuBSSN_s**  
**619.lbm_s**  
**621.wrf_s**  
**627.cam4_s**  
**628.pop2_s**  
**638.imagick_s**  
**644.nab_s**  
**649.fotonik3d_s**  
**654.roms_s**

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
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<tr>
<td>155</td>
<td>156</td>
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</table>

#### SPECspeed Benchmark Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>SPECspeed®2017_fp_base</th>
<th>SPECspeed®2017_fp_peak</th>
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<td>bwaves_s</td>
<td>189</td>
<td>188</td>
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<tr>
<td>cactuBSSN_s</td>
<td>107</td>
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<tr>
<td>lbm_s</td>
<td>131</td>
<td>137</td>
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<tr>
<td>wrf_s</td>
<td>122</td>
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<tr>
<td>cam4_s</td>
<td>63.5</td>
<td>63.5</td>
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<tr>
<td>pop2_s</td>
<td>168</td>
<td>176</td>
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<tr>
<td>imagick_s</td>
<td>318</td>
<td>318</td>
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<tr>
<td>nab_s</td>
<td>86.5</td>
<td>86.9</td>
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<tr>
<td>fotoni3d_s</td>
<td>158</td>
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</tbody>
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SPEC CPU®2017 Floating Point Speed Result

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Hewlett Packard Enterprise
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Synergy 480 Gen10
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SPECspeed®2017_fp_base = 155
SPECspeed®2017_fp_peak = 156

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Jan-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<td>603.bwaves_s</td>
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<td>607.cactuBSSN_s</td>
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<td>88.3</td>
<td>189</td>
<td>88.8</td>
<td>188</td>
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<td>48.7</td>
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<td>628.pop2_s</td>
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<td>187</td>
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<tr>
<td>649.fotonik3d_s</td>
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<td>654.roms_s</td>
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<td>162</td>
<td>98.7</td>
<td>159</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Hewlett Packard Enterprise
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Synergy 480 Gen10
(2.70 GHz, Intel Xeon Gold 6258R)

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SPECspeed®2017_fp_peak = 156

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: Jan-2020
Hardware Availability: Feb-2020
Software Availability: Jun-2019

Platform Notes

BIOS Configuration:
Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Peak Frequency Compute
Minimum Processor Idle Power Core C-State set to C1E State
Energy/Performance Bias set to Balanced Power
Workload Profile set to Custom
Numa Group Size Optimization set to Flat
Advanced Memory Protection set to Advanced ECC

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbe6e46a485a0011
running on sy480-sles15sp1-hs Fri Jan 24 06:50:12 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6258R CPU @ 2.70GHz
2 "physical id"s (chips)
56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
Address sizes: 46 bits physical, 48 bits virtual
CPU(s): 56
On-line CPU(s) list: 0-55
Thread(s) per core: 1
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel

(Continued on next page)
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Platform Notes (Continued)

CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6258R CPU @ 2.70GHz
Stepping: 7
CPU MHz: 2700.000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 39424K
NUMA node0 CPU(s): 0-27
NUMA node1 CPU(s): 28-55

Flags: fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperf perfctr pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_ppin ssbd mba ibrs ibpb stibp ibrs_enhanced tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ets invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves xsavec xgetbv1 xsaves cqm_llc cqm_occap_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pku ospke avx512_vnni md_clear flush_lld

/arch_capabilities

/proc/cpuinfo cache data
  cache size: 39424 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
node 0 size: 193023 MB
node 0 free: 192352 MB
node 1 cpus: 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55
node 1 size: 193348 MB
node 1 free: 193032 MB
node distances:
  node 0 1
  0: 10 21
  1: 21 10

From /proc/meminfo
MemTotal: 395645124 kB
 HugePages_Total: 0

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Platform Notes (Continued)

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
    NAME="SLES"
    VERSION="15-SP1"
    VERSION_ID="15.1"
    PRETTY_NAME="SUSE Linux Enterprise Server 15 SP1"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15:sp1"

uname -a:
    Linux sy480-sles15sp1-hs 4.12.14-195-default #1 SMP Tue May 7 10:55:11 UTC 2019
    (8fba516) x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: Not affected
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
    via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional,
    RSB filling

run-level 3 Jan 24 06:48

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sda4 xfs 143G 19G 125G 13% /home

From /sys/devices/virtual/dmi/id
    BIOS: HPE I42 12/10/2019
    Vendor: HPE
    Product: Synergy 480 Gen10
    Product Family: Synergy
    Serial: MXQ72204FC

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory:
    24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933

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**Platform Notes (Continued)**

(End of data from sysinfo program)

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**Compiler Version Notes**

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<th>Test Sponsor</th>
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<th>Software Availability</th>
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<tr>
<td>Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td>HPE</td>
<td>Feb-2020</td>
<td>Jun-2019</td>
</tr>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416</td>
<td>HPE</td>
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

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CPU\textsuperscript{2017} License: & 3 \\
Test Sponsor: & HPE \\
Tested by: & HPE \\
\hline
\end{tabular}

Test Date: Jan-2020  
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\section*{Base Optimization Flags (Continued)}

Benchmarks using both Fortran and C:
\begin{itemize}
\item -xCORE-AVX512
\item -ipo
\item -03
\item -no-prec-div
\item -qopt-prefetch
\item -ffinite-math-only
\item -qopt-mem-layout-trans=4
\item -qopenmp
\item -DSPEC\_OPENMP
\item -nostandard-realloc-lhs
\end{itemize}

Benchmarks using Fortran, C, and C++:
\begin{itemize}
\item -xCORE-AVX512
\item -ipo
\item -03
\item -no-prec-div
\item -qopt-prefetch
\item -ffinite-math-only
\item -qopt-mem-layout-trans=4
\item -qopenmp
\item -DSPEC\_OPENMP
\item -nostandard-realloc-lhs
\end{itemize}

\section*{Peak Compiler Invocation}

\begin{itemize}
\item C benchmarks:  
  icc -m64 -std=c11
\item Fortran benchmarks:  
  ifort -m64
\item Benchmarks using both Fortran and C:  
  ifort -m64 icc -m64 -std=c11
\item Benchmarks using Fortran, C, and C++:  
  icpc -m64 icc -m64 -std=c11 ifort -m64
\end{itemize}

\section*{Peak Portability Flags}

Same as Base Portability Flags

\section*{Peak Optimization Flags}

\begin{itemize}
\item C benchmarks:  
  -xCORE-AVX512
\item -ipo
\item -03
\item -no-prec-div
\item -qopt-prefetch
\item -ffinite-math-only
\item -qopt-mem-layout-trans=4
\item -qopenmp
\item -DSPEC\_OPENMP
\end{itemize}

\begin{itemize}
\item Fortran benchmarks:  
  603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC\_SUPPRESS\_OPENMP
  -DSPEC\_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -03
\end{itemize}

(Continued on next page)
Peak Optimization Flags (Continued)

603.bwaves_s (continued):
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

628.pop2_s: Same as 621.wrf_s

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html
http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.2019-04-03.00.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml
http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.2019-04-03.00.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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