## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**
Cisco UCS C480 M5 (Intel Xeon Gold 6248, 2.50GHz)

<table>
<thead>
<tr>
<th>Thread</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s 80</td>
<td>8.94</td>
<td>10.4</td>
</tr>
<tr>
<td>602.gcc_s 80</td>
<td>8.24</td>
<td>10.2</td>
</tr>
<tr>
<td>605.mcf_s 80</td>
<td>8.35</td>
<td>10.2</td>
</tr>
<tr>
<td>620.omnetpp_s 80</td>
<td>8.24</td>
<td>10.2</td>
</tr>
<tr>
<td>623.xalancbmk_s 80</td>
<td>12.4</td>
<td>12.4</td>
</tr>
<tr>
<td>625.x264_s 80</td>
<td>14.5</td>
<td>14.5</td>
</tr>
<tr>
<td>641.leela_s 80</td>
<td>4.78</td>
<td>4.78</td>
</tr>
<tr>
<td>648.exchange2_s 80</td>
<td>16.7</td>
<td>16.7</td>
</tr>
<tr>
<td>657.xz_s 80</td>
<td>25.0</td>
<td>25.1</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Gold 6248
- **Max MHz:** 3900
- **Nominal:** 2500
- **Enabled:** 80 cores, 4 chips
- **Orderable:** 2.4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 27.5 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Desktop 15 (x86_64) 4.12.14-23-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4i released Aug-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<th>Ratio</th>
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</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
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<td>6.81</td>
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<td>6.79</td>
<td>260</td>
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<td>222</td>
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<td>223</td>
<td>7.96</td>
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<td>393</td>
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<td>12.4</td>
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<tr>
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<tr>
<td>631.deepsjeng_s</td>
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<tr>
<td>648.exchange2_s</td>
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<td>176</td>
<td>16.7</td>
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<tr>
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<td>24.9</td>
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<td>25.0</td>
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<td>25.1</td>
<td>247</td>
<td>25.1</td>
<td></td>
</tr>
</tbody>
</table>

| SPECspec®2017_int_base | = 10.2 |
| SPECspec®2017_int_peak  | = 10.4 |

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

SPEC CPU®2017 Integer Speed Result

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6248, 2.50GHz)

SPECspeed®2017_int_base = 10.2
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Disabled
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
running on linux-3zzzh Thu Feb  6 12:25:35 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
 4 "physical id"s (chips)
80 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 20
siblings : 20
  physical 0: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  physical 1: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  physical 2: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28
  physical 3: cores 0 1 2 3 4 8 9 10 11 12 16 17 18 19 20 24 25 26 27 28

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 80
On-line CPU(s) list: 0-79
Thread(s) per core: 1
Core(s) per socket: 20
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
Stepping: 6
CPU MHz: 2500.000
CPU max MHz: 3900.000
CPU min MHz: 1000.000
BogoMIPS: 5000.00
Virtualization: VT-x

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6248, 2.50GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

**SPECCPU®2017 Integer Speed Result**

**SPECspeed®2017_int_base = 10.2**
**SPECspeed®2017_int_peak = 10.4**

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**Platform Notes (Continued)**

```
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 28160K
NUMA node0 CPU(s): 0-19
NUMA node1 CPU(s): 20-39
NUMA node2 CPU(s): 40-59
NUMA node3 CPU(s): 60-79

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_pcin mba tpr_shadow vnumi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsavesopt xsavec xgetbv1 xsavec_cqm xmm_cqm_cqm_total cqm_mbb_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size : 28160 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
  physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
  node 0 size: 385626 MB
  node 1 cpus: 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
  node 1 size: 387057 MB
  node 1 free: 386639 MB
  node 2 cpus: 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59
  node 2 size: 387057 MB
  node 2 free: 386843 MB
  node 3 cpus: 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79
  node 3 size: 387026 MB
  node 3 free: 386778 MB
  node distances:
    node 0 1 2 3
      0: 10 21 21 21
      1: 21 10 21 21
      2: 21 21 10 21
      3: 21 21 21 10

From /proc/meminfo
```

(Continued on next page)
Cisco Systems
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SPECspeed®2017_int_base = 10.2
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

MemTotal: 1583890224 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLED"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Desktop 15"
    ID="sled"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sled:15"

uname -a:
  Linux linux-3zzh 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Feb 6 12:25

SPEC is set to: /home/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda2 btrfs 893G 10G 882G 2% /home

From /sys/devices/virtual/dmi/id
  BIOS: Cisco Systems, Inc. C480M5.4.0.4i.0.0831191123 08/31/2019
  Vendor: Cisco Systems Inc
  Product: UCSC-C480-M5
  Serial: FCH2243W038

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  Memory:

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6248, 2.50GHz)

SPEC CPU®2017 Integer Speed Result
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SPECspeed®2017_int_base = 10.2
SPECspeed®2017_int_peak = 10.4

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6248, 2.50GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934
(End of data from sysinfo program)

Compiler Version Notes

C
600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++
620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran
648.exchange2_s(base, peak)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6248, 2.50GHz)

SPECspeed®2017_int_base = 10.2
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Portability Flags
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

Peak Compiler Invocation
C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6248, 2.50GHz)

SPECspeed®2017_int_base = 10.2
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-\L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-\L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -qopt-mem-layout-trans=4 -no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-\L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-\L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -\L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-\L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-\L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

(Continued on next page)
Cisco Systems
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SPECspeed®2017_int_base = 10.2
SPECspeed®2017_int_peak = 10.4

CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Test Date: Feb-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags (Continued)

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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