SPEC CPU®2017 Floating Point Speed Result

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Cisco Systems

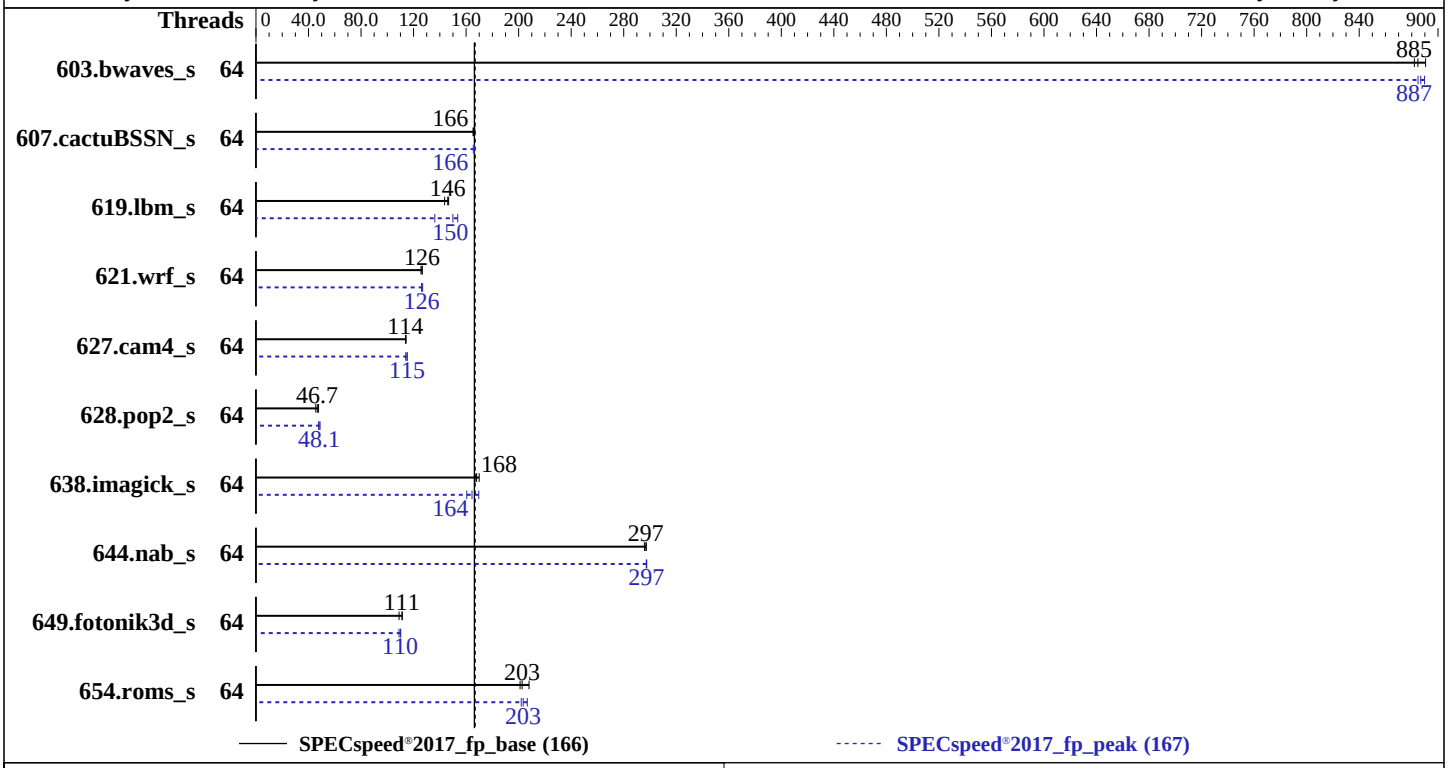
Cisco UCS B480 M5 (Intel Xeon Gold 5218, 2.30GHz)

SPECspeed®2017_fp_base = 166

SPECspeed®2017_fp_peak = 167

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2020
Hardware Availability: Apr-2019
Software Availability: May-2019



Hardware

CPU Name:	Intel Xeon Gold 5218
Max MHz:	3900
Nominal:	2300
Enabled:	64 cores, 4 chips
Orderable:	2,4 Chips
Cache L1:	32 KB I + 32 KB D on chip per core
L2:	1 MB I+D on chip per core
L3:	22 MB I+D on chip per chip
Other:	None
Memory:	1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
Storage:	1 x 1.9 TB SSD SAS
Other:	None

Software

OS:	SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler:	C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel:	Yes
Firmware:	Version 4.0.4b released Apr-2019
File System:	btrfs
System State:	Run level 3 (multi-user)
Base Pointers:	64-bit
Peak Pointers:	64-bit
Other:	None
Power Management:	BIOS set to prefer performance at the cost of additional power usage

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Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	64	**66.7**	**885**	66.9	882	66.2	891	64	**66.5**	**887**	66.3	890	66.7	885
607.cactuBSSN_s	64	100	167	**101**	**166**	101	165	64	101	165	100	166	**100**	**166**
619.lbm_s	64	36.5	144	35.7	147	**35.9**	**146**	64	34.1	154	**34.9**	**150**	38.5	136
621.wrf_s	64	**105**	**126**	104	127	105	126	64	105	126	**105**	**126**	104	127
627.cam4_s	64	77.5	114	**77.8**	**114**	77.9	114	64	77.7	114	76.9	115	**77.0**	**115**
628.pop2_s	64	249	47.7	261	45.5	**254**	**46.7**	64	243	48.8	**247**	**48.1**	249	47.7
638.imagick_s	64	**85.9**	**168**	84.9	170	86.2	167	64	**87.7**	**164**	85.0	170	89.9	161
644.nab_s	64	59.1	296	58.8	297	**58.9**	**297**	64	58.8	297	58.7	298	**58.8**	**297**
649.fotonik3d_s	64	**82.0**	**111**	83.7	109	81.8	111	64	82.7	110	**82.9**	**110**	83.7	109
654.roms_s	64	**77.7**	**203**	75.7	208	78.3	201	64	76.2	207	78.0	202	**77.4**	**203**

SPECspeed®2017_fp_base = 166

SPECspeed®2017_fp_peak = 167

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"
```

General Notes

```
 Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
 memory using Redhat Enterprise Linux 7.5
 Transparent Huge Pages enabled by default
 Prior to runcpu invocation
 Filesystem page cache synced and cleared with:
 sync; echo 3>       /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
```

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6365 of 2019-08-21 295195f888a3d7edb1e6e46a485a0011
 running on linux-icbf Mon Jan 20 10:35:45 2020

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
       4  "physical id"s (chips)
       64 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 16
       siblings  : 16
       physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 2: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
       physical 3: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

 From lscpu:
      Architecture:        x86_64
      CPU op-mode(s):      32-bit, 64-bit
      Byte Order:          Little Endian
      CPU(s):              64
      On-line CPU(s) list: 0-63
      Thread(s) per core:  1
      Core(s) per socket:  16
      Socket(s):           4
      NUMA node(s):        4
      Vendor ID:           GenuineIntel
      CPU family:          6
      Model:               85
      Model name:          Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
      Stepping:            6
      CPU MHz:             2300.000
      CPU max MHz:         3900.0000
      CPU min MHz:         1000.0000
      BogoMIPS:            4600.00
      Virtualization:      VT-x
```

(Continued on next page)

Platform Notes (Continued)

```
      L1d cache:             32K
      L1i cache:             32K
      L2 cache:              1024K
      L3 cache:              22528K
      NUMA node0 CPU(s):     0-15
      NUMA node1 CPU(s):     16-31
      NUMA node2 CPU(s):     32-47
      NUMA node3 CPU(s):     48-63
      Flags:                 fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
      pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
      lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
      aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
      sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
      tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
      epb cat_l3 cdp_l3 invpcid_single intel_ppin mba tpr_shadow vnmi flexpriority ept
      vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
      avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
      xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
      ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
      ospke avx512_vnni arch_capabilities ssbd

 /proc/cpuinfo cache data
    cache size : 22528 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
   available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
   node 0 size: 385627 MB
   node 0 free: 385291 MB
   node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
   node 1 size: 387058 MB
   node 1 free: 379862 MB
   node 2 cpus: 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
   node 2 size: 387058 MB
   node 2 free: 386558 MB
   node 3 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
   node 3 size: 387026 MB
   node 3 free: 386789 MB
   node distances:
   node   0   1   2   3
     0:  10  21  31  21
     1:  21  10  21  31
     2:  31  21  10  21
     3:  21  31  21  10

 From /proc/meminfo
```

(Continued on next page)

Platform Notes (Continued)

```
    MemTotal:       1583893680 kB
    HugePages_Total:       0
    Hugepagesize:       2048 kB

  From /etc/*release* /etc/*version*
    os-release:
       NAME="SLES"
       VERSION="15"
       VERSION_ID="15"
       PRETTY_NAME="SUSE Linux Enterprise Server 15"
       ID="sles"
       ID_LIKE="suse"
       ANSI_COLOR="0;32"
       CPE_NAME="cpe:/o:suse:sles:15"

  uname -a:
    Linux linux-icbf 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

  Kernel self-reported vulnerability status:

  CVE-2018-3620 (L1 Terminal Fault):        No status reported
  Microarchitectural Data Sampling:         No status reported
  CVE-2017-5754 (Meltdown):                 Not affected
  CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                            via prctl and seccomp
  CVE-2017-5753 (Spectre variant 1):        Mitigation: __user pointer sanitization
  CVE-2017-5715 (Spectre variant 2):        Mitigation: Indirect Branch Restricted
                                            Speculation, IBPB, IBRS_FW

  run-level 3 Jan 20 05:54

  SPEC is set to: /home/cpu2017
    Filesystem     Type   Size  Used Avail Use% Mounted on
    /dev/sdb2      btrfs  222G   15G  207G   7% /home

  From /sys/devices/virtual/dmi/id
      BIOS:    Cisco Systems, Inc. B480M5.4.0.4b.0.0407190454 04/07/2019
      Vendor:  Cisco Systems Inc
      Product: UCSB-B480-M5
      Serial:  FLM230102QU

  Additional information from dmidecode follows.  WARNING: Use caution when you interpret
  this section. The 'dmidecode' program reads system data which is "intended to allow
  hardware to be accurately determined", but the intent may not be met, as there are
  frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    Memory:
```

(Continued on next page)

Platform Notes (Continued)

```
     48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

  (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
                | 644.nab_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
                | 654.roms_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
                | 628.pop2_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
```

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Compiler Version Notes (Continued)

```
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

Fortran benchmarks:
`ifort -m64`

Benchmarks using both Fortran and C:
`ifort -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
`icpc -m64 icc -m64 -std=c11 ifort -m64`

Base Portability Flags

603.bwaves_s: `-DSPEC_LP64`
607.cactuBSSN_s: `-DSPEC_LP64`
619.lbm_s: `-DSPEC_LP64`
621.wrf_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
627.cam4_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
628.pop2_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl`
638.imagick_s: `-DSPEC_LP64`
644.nab_s: `-DSPEC_LP64`
649.fotonik3d_s: `-DSPEC_LP64`
654.roms_s: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`

Fortran benchmarks:
`-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`

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Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:

(Continued on next page)

Peak Optimization Flags (Continued)

603.bwaves_s: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs`

649.fotonik3d_s: `Same as 603.bwaves_s`

654.roms_s: `-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs`

Benchmarks using both Fortran and C:

621.wrf_s: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`

627.cam4_s: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`

628.pop2_s: `Same as 621.wrf_s`

Benchmarks using Fortran, C, and C++:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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