**SPEC CPU®2017 Integer Speed Result**

**Cisco Systems**  
Cisco UCS B480 M5 (Intel Xeon Platinum 8268, 2.90GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base = 10.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak = 10.7</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jan-2020  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

<table>
<thead>
<tr>
<th><strong>Threads</strong></th>
<th>SPECspeed®2017_int_base (10.4)</th>
<th>SPECspeed®2017_int_peak (10.7)</th>
</tr>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>96</td>
<td>6.84</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>96</td>
<td>9.98</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>96</td>
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</tr>
<tr>
<td>620.omnetpp_s</td>
<td>96</td>
<td>9.25</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>96</td>
<td>9.38</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>96</td>
<td>12.4</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>96</td>
<td>14.6</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>96</td>
<td>14.7</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>96</td>
<td>16.7</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>96</td>
<td>24.0</td>
</tr>
</tbody>
</table>

**Hardware**

- **CPU Name:** Intel Xeon Platinum 8268  
- **Max MHz:** 3900  
- **Nominal:** 2900  
- **Enabled:** 96 cores, 4 chips  
- **Orderable:** 2.4 Chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **L2:** 1 MB I+D on chip per core  
- **L3:** 35.75 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)  
- **Storage:** 1 x 1.9 TB SSD SAS  
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
- **Parallel:** Yes  
- **Firmware:** Version 4.0.4b released Apr-2019  
- **File System:** btrfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** 64-bit  
- **Other:** jemalloc memory allocator V5.0.1  
- **Power Management:** BIOS set to prefer performance at the cost of additional power usage
## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
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<tbody>
<tr>
<td>600.perlbench_s</td>
<td>96</td>
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<td>12.4</td>
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<tr>
<td>625.x264_s</td>
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<td>14.7</td>
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<td>16.7</td>
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<td>24.6</td>
<td></td>
<td>252</td>
<td>24.5</td>
<td>252</td>
<td>24.6</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

## Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

## Environment Variables Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
- OMP_STACKSIZE = "192M"

## General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3 > /proc/sys/vm/drop_caches
```

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

jemalloc, a general purpose malloc implementation built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Sources available from jemalloc.net or https://github.com/jemalloc/jemalloc/releases
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPEC SPEED®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7eddb1e6e46a485a0011
running on linux-db10 Wed Jan 8 15:03:15 2020

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

model name: Intel(R) Xeon(R) Platinum 8268 CPU @ 2.90GHz
4 "physical id"s (chips)
96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores: 24
siblings: 24
physical 0: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 3: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8268 CPU @ 2.90GHz
Stepping: 6
CPU MHz: 2900.000
CPU max MHz: 3900.0000
CPU min MHz: 1200.0000
BogoMIPS: 5800.00
Virtualization: VT-x

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPECspeak®2017_int_base = 10.4
SPECspeak®2017_int_peak = 10.7

Platform Notes (Continued)

| L1d cache: | 32K |
| L1i cache: | 32K |
| L2 cache: | 1024K |
| L3 cache: | 36608K |
| NUMA node0 CPU(s): | 0-23 |
| NUMA node1 CPU(s): | 24-47 |
| NUMA node2 CPU(s): | 48-71 |
| NUMA node3 CPU(s): | 72-95 |

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 cklflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdmb fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cpd_l3 invpcid_single intel_pmm mba tpr_shadow vnumi flexpriority ept
vpid fsbgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erts invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx dpms clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsavec xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbm_local
ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku
ospke avx512_vnni arch_capabilities ssbd

From /proc/cpuinfo cache data
  cache size: 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
  node 0 size: 385596 MB
  node 0 free: 385043 MB
  node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
  node 1 size: 387056 MB
  node 1 free: 386857 MB
  node 2 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
  node 2 size: 387056 MB
  node 2 free: 386862 MB
  node 3 cpus: 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
  node 3 size: 387054 MB
  node 3 free: 386858 MB
  node distances:
    node 0 1 2 3
    0: 10 21 21 21
    1: 21 10 21 21
    2: 21 21 10 21
    3: 21 21 21 10

From /proc/meminfo

(Continued on next page)
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.7

Platform Notes (Continued)

MemTotal: 1583887508 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-db10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
  via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted
Speculation, IBPB, IBRS_FW

run-level 3 Jan 8 15:00

SPEC is set to: /home/cpu2017
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda2 btrfs 222G 64G 157G 30% /home

From /sys/devices/virtual/dmi/id
  BIOS: Cisco Systems, Inc. B480M5.4.0.4b.0.0407190454 04/07/2019
  Vendor: Cisco Systems Inc
  Product: UCSB-B480-M5
  Serial: FLM225202G1

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

Memory:
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPEC CPU®2017 Integer Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.7

CPU2017 License: 9019
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Tested by: Cisco Systems

Test Date: Jan-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

C

| 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak) |

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++

| 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak) |

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran

| 648.exchange2_s(base, peak) |

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Jan-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Portability Flags
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

Peak Compiler Invocation
C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64
Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Platinum 8268, 2.90GHz)

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.7

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Jan-2020
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-LL/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-LL/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-LL/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-LL/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-LL/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-LL/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

(Continued on next page)
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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Peak Optimization Flags (Continued)

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.1.0 on 2020-01-08 18:03:14-0500.
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