Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5220, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>162</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>162</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

| Threads | 0  | 40.0 | 80.0 | 120 | 160 | 200 | 240 | 280 | 320 | 360 | 400 | 440 | 480 | 520 | 560 | 600 | 640 | 680 | 720 | 760 | 800 | SPECspeed®2017_fp_base (162) |
|---------|----|------|------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 603.bwaves_s | 72 | 810 | 810 | 171 |
| 607.cactuBSSN_s | 72 | 171 | 171 | 146 |
| 619.lbm_s | 72 | 141 | 141 | 126 |
| 621.wrf_s | 72 | 125 | 125 | 127 |
| 627.cam4_s | 72 | 128 | 128 | 51.5 |
| 628.pop2_s | 72 | 51.7 | 51.7 | 182 |
| 638.imagick_s | 72 | 182 | 182 | 315 |
| 644.nab_s | 72 | 315 | 315 | 108 |
| 649.fotonik3d_s | 72 | 107 | 107 | 121 |
| 654.roms_s | 72 | 121 | 121 | 121 |

Hardware

CPUs: 1 Intel Xeon Gold 5220  
Max MHz: 3900  
Nominal: 2200  
Enabled: 72 cores, 4 chips  
Orderable: 2.4 Chips  
Cache L1: 32 KB I + 32 KB D on chip per core  
L2: 1 MB I+D on chip per core  
L3: 24.75 MB I+D on chip per chip  
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)  
Storage: 1 x 960 GB SSD SAS  
Other: None

Software

OS: SUSE Linux Enterprise Desktop 15 (x86_64)  
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux  
Parallel: Yes  
Firmware: Version 4.0.4i released Aug-2019  
File System: btrfs  
System State: Run level 3 (multi-user)  
Base Pointers: 64-bit  
Peak Pointers: 64-bit  
Other: None  
Power Management: BIOS set to prefer performance at the cost of additional power usage
SPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5220, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

SPECspeed®2017_fp_base = 162
SPECspeed®2017_fp_peak = 162

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>72</td>
<td>72.5</td>
<td>814</td>
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<td>811</td>
<td>74.0</td>
<td>797</td>
<td>72</td>
<td>72.6</td>
<td>812</td>
<td>73.4</td>
<td>803</td>
<td>72.8</td>
<td>810</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>72</td>
<td>97.5</td>
<td>171</td>
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<td>97.7</td>
<td>171</td>
<td>72</td>
<td>97.2</td>
<td>171</td>
<td>96.9</td>
<td>172</td>
<td>97.2</td>
<td>171</td>
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<tr>
<td>619.llm_s</td>
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<td>36.0</td>
<td>146</td>
<td>36.5</td>
<td>143</td>
<td>35.8</td>
<td>146</td>
<td>72</td>
<td>37.3</td>
<td>140</td>
<td>37.1</td>
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<tr>
<td>621.wrf_s</td>
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<td>105</td>
<td>126</td>
<td>105</td>
<td>127</td>
<td>105</td>
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<td>628.pop2_s</td>
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<td>230</td>
<td>51.5</td>
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<td>72</td>
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<td>51.7</td>
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<td>52.3</td>
<td>230</td>
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<td>638.imagick_s</td>
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<td>182</td>
<td>82.0</td>
<td>176</td>
</tr>
<tr>
<td>644.nab_s</td>
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<td>55.5</td>
<td>315</td>
<td>55.4</td>
<td>315</td>
<td>55.5</td>
<td>315</td>
<td>72</td>
<td>55.7</td>
<td>314</td>
<td>55.5</td>
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<td>55.5</td>
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<tr>
<td>649.fotonik3d_s</td>
<td>72</td>
<td>85.2</td>
<td>107</td>
<td>83.7</td>
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<td>84.1</td>
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<td>83.7</td>
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<td>85.3</td>
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<td>85.2</td>
<td>107</td>
</tr>
<tr>
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<td>72</td>
<td>125</td>
<td>126</td>
<td>130</td>
<td>121</td>
<td>130</td>
<td>121</td>
<td>72</td>
<td>127</td>
<td>124</td>
<td>130</td>
<td>121</td>
<td>136</td>
<td>116</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
## Platform Notes

**BIOS Settings:**
Intel HyperThreading Technology set to Disabled  
CPU performance set to Enterprise

**SNC set to Disabled**
Patrol Scrub set to Disabled

### Sysinfo program
/home/cpu2017/bin/sysinfo  
Rev: r6365 of 2019-08-21 295195f888a3d7ed3b36e46a485a0011  
running on linux-3zzh Wed Dec 25 14:11:24 2019

**SUT (System Under Test) info as seen by some common utilities.**  
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From `/proc/cpuinfo`

- **model name**: Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz
  - 4 "physical id"s (chips)
  - 72 "processors"
- **cores, siblings** (Caution: counting these is hw and system dependent. The following excerpts from `/proc/cpuinfo` might not be reliable. Use with caution.)
  - cpu cores : 18
  - siblings : 18
  - physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  - physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  - physical 2: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  - physical 3: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From `lscpu`

- **Architecture**: x86_64  
- **CPU op-mode(s)**: 32-bit, 64-bit  
- **Byte Order**: Little Endian  
- **CPU(s)**: 72  
- **On-line CPU(s) list**: 0-71  
- **Thread(s) per core**: 1  
- **Core(s) per socket**: 18  
- **Socket(s)**: 4  
- **NUMA node(s)**: 4  
- **Vendor ID**: GenuineIntel  
- **CPU family**: 6  
- **Model**: 85  
- **Model name**: Intel(R) Xeon(R) Gold 5220 CPU @ 2.20GHz  
- **Stepping**: 6  
- **CPU MHz**: 2200.000  
- **CPU max MHz**: 3900.0000  
- **CPU min MHz**: 1000.0000  
- **BogoMIPS**: 4400.00

(Continued on next page)
## Cisco Systems

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### CPU2017 License:
9019

### Test Sponsor:
Cisco Systems

### Tested by:
Cisco Systems

### Software Availability:
May-2019

### Hardware Availability:
Apr-2019

### Test Date:
Dec-2019

---

### Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Virtualization:</th>
<th>VT-x</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>25344K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-17</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>18-35</td>
</tr>
<tr>
<td>NUMA node2 CPU(s):</td>
<td>36-53</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
<td>54-71</td>
</tr>
<tr>
<td>Flags:</td>
<td>fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 cdp_13 invpcid_single intel_ppi maa tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdtsa avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xSAVE xSaves cmq_llc cmq_occup llc cmq_mbb total cmq_mbb local lsb ibp bb ibts stibp dtherm iaxl pdn pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospe avx512_vnni arch_capabilities ssbd</td>
</tr>
</tbody>
</table>

From `numactl --hardware`

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
```

Available: 4 nodes (0-3)

- Node 0:
  - CPUs: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
  - Size: 385626 MB
  - Free: 385105 MB

- Node 1:
  - CPUs: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
  - Size: 387058 MB
  - Free: 386702 MB

- Node 2:
  - CPUs: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
  - Size: 387058 MB
  - Free: 379411 MB

- Node 3:
  - CPUs: 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
  - Size: 387026 MB
  - Free: 386707 MB

Node distances:

- Node 0:
  - 0: 1 2 3
  - 1: 21 10 31 21
  - 2: 21 31 10 21
  - 3: 31 21 21 10

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5220, 2.20GHz)

SPEC CPU®2017 Floating Point Speed Result
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Platform Notes (Continued)

From /proc/meminfo
MemTotal:      1583891764 kB
HugePages_Total:       0
Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
    NAME="SLED"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Desktop 15"
    ID="sled"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sled:15"

uname -a:
    Linux linux-3zzh 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2018-3620 (L1 Terminal Fault):        No status reported
Microarchitectural Data Sampling:         No status reported
CVE-2017-5754 (Meltdown):                 Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                              via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):        Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):        Mitigation: Indirect Branch Restricted
                                              Speculation, IBPB, IBRS_FW

run-level 3 Dec 25 09:35
SPEC is set to: /home/cpu2017
    Filesystem  Type       Size  Used  Avail Use% Mounted on
    /dev/sda2    btrfs      893G   16G  876G   2%   /home

From /sys/devices/virtual/dmi/id
    BIOS:    Cisco Systems, Inc. C480M5.4.0.4i.0.0831191123 08/31/2019
    Vendor:  Cisco Systems Inc
    Product: UCSC-C480-M5
    Serial:  FCH2243W038

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
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Cisco UCS C480 M5 (Intel Xeon Gold 5220, 2.20GHz)  

SPEC CPU®2017 Floating Point Speed Result

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SPECspeed®2017_fp_base = 162
SPECspeed®2017_fp_peak = 162

Platform Notes (Continued)

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C              | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
              | 644.nab_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Compiler Version Notes

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Compiler Version Notes

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
              | 654.roms_s(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
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Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Compiler Version Notes

==============================================================================
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
              | 628.pop2_s(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
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Compiler Version Notes (Continued)

Intel (R) C Intel (R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch

(Continued on next page)
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### Base Optimization Flags (Continued)

- Fortran benchmarks (continued):
  - `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp`
  - `-nostandard-realloc-lhs`

- Benchmarks using both Fortran and C:
  - `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
  - `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`
  - `-nostandard-realloc-lhs`

- Benchmarks using Fortran, C, and C++:
  - `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
  - `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`
  - `-nostandard-realloc-lhs`

### Peak Compiler Invocation

- C benchmarks:
  - `icc -m64 -std=c11`

- Fortran benchmarks:
  - `ifort -m64`

- Benchmarks using both Fortran and C:
  - `ifort -m64 icc -m64 -std=c11`

- Benchmarks using Fortran, C, and C++:
  - `icpc -m64 icc -m64 -std=c11 ifort -m64`

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

C benchmarks:
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`

Fortran benchmarks:

(Continued on next page)
## Peak Optimization Flags (Continued)

### 603. bwaves_s:
- `--prof-gen(pass 1) --prof-use(pass 2) --DSPEC_SUPPRESS_OPENMP`
- `--DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3`
- `--ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4`
- `--qopenmp -nostandard-realloc-lhs`

`649.fotonik3d_s`: Same as `603.bwaves_s`

### 654. roms_s:
- `--DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `--ffinite-math-only -qopt-mem-layout-trans=4`
- `--qopenmp -nostandard-realloc-lhs`

### Benchmarks using both Fortran and C:

### 621. wrf_s:
- `--prof-gen(pass 1) --prof-use(pass 2) -O2 -xCORE-AVX512`
- `--qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4`
- `--DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`

### 627. cam4_s:
- `--xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `--ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`

### 628. pop2_s:
- Same as `621.wrf_s`

### Benchmarks using Fortran, C, and C++:
- `--xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`
- `--ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links: