SPEC CPU®2017 Floating Point Speed Result

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Cisco Systems

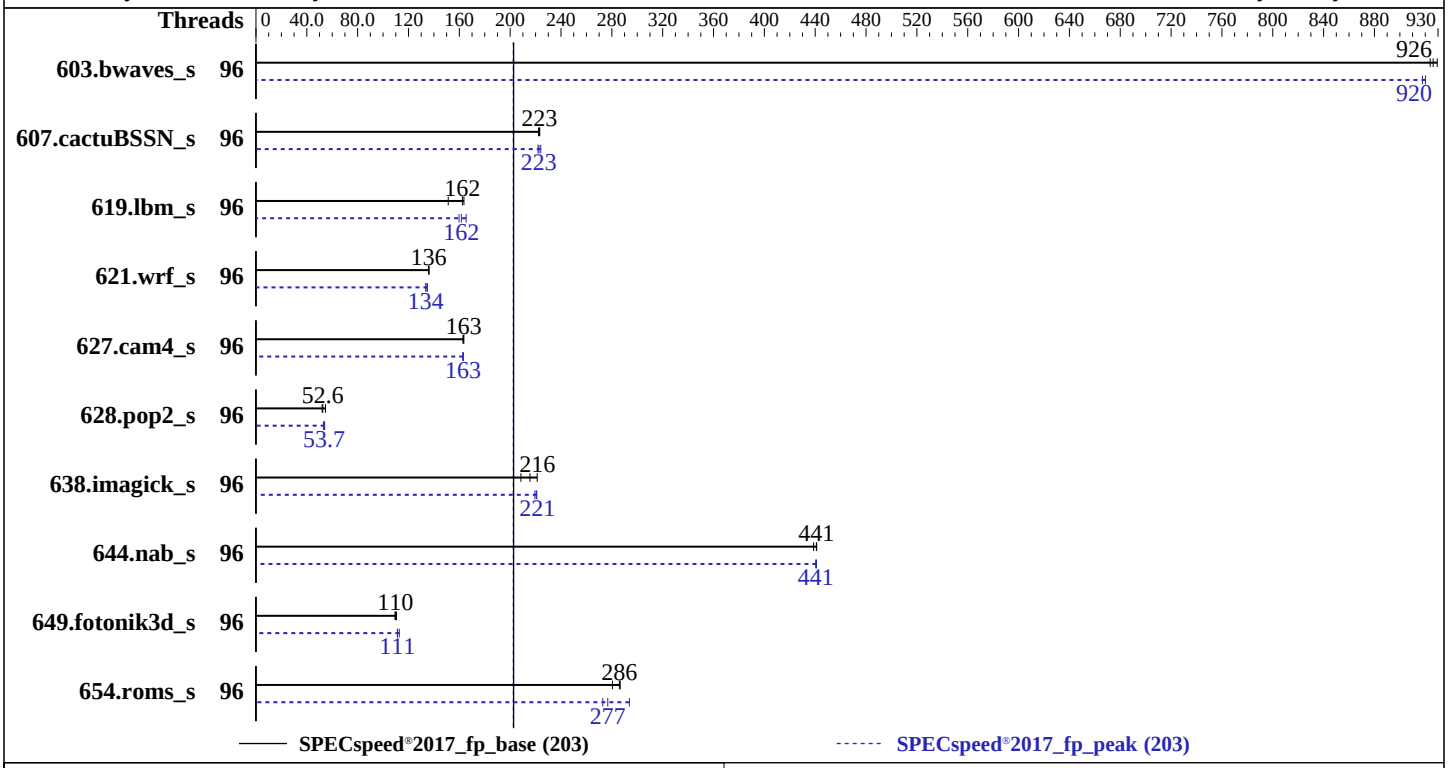
Cisco UCS C480 M5 (Intel Xeon Platinum 8260L, 2.40GHz)

SPECspeed®2017_fp_base = 203

SPECspeed®2017_fp_peak = 203

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Nov-2019
Hardware Availability: Apr-2019
Software Availability: May-2019



Hardware

CPU Name:	Intel Xeon Platinum 8260L
Max MHz:	3900
Nominal:	2400
Enabled:	96 cores, 4 chips
Orderable:	2,4 Chips
Cache L1:	32 KB I + 32 KB D on chip per core
L2:	1 MB I+D on chip per core
L3:	35.75 MB I+D on chip per chip
Other:	None
Memory:	1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
Storage:	1 x 1.9 TB SSD SAS
Other:	None

Software

OS:	SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
Compiler:	C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel:	Yes
Firmware:	Version 4.0.3 released Mar-2019
File System:	xfs
System State:	Run level 3 (multi-user)
Base Pointers:	64-bit
Peak Pointers:	64-bit
Other:	None
Power Management:	BIOS set to prefer performance at the cost of additional power usage

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Results Table

Benchmark	Base							Peak						
	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio	Threads	Seconds	Ratio	Seconds	Ratio	Seconds	Ratio
603.bwaves_s	96	**63.7**	**926**	63.5	929	63.9	924	96	64.1	920	**64.1**	**920**	64.3	918
607.cactuBSSN_s	96	74.7	223	75.0	222	**74.7**	**223**	96	74.4	224	75.1	222	**74.9**	**223**
619.lbm_s	96	32.0	164	**32.2**	**162**	34.6	151	96	31.7	165	**32.4**	**162**	32.8	160
621.wrf_s	96	97.4	136	97.2	136	**97.2**	**136**	96	99.0	134	**98.9**	**134**	98.0	135
627.cam4_s	96	54.2	163	**54.2**	**163**	54.4	163	96	**54.4**	**163**	54.4	163	54.3	163
628.pop2_s	96	**226**	**52.6**	217	54.7	228	52.1	96	224	53.1	220	54.0	**221**	**53.7**
638.imagick_s	96	69.2	208	**66.9**	**216**	65.2	221	96	65.3	221	**65.4**	**221**	65.7	219
644.nab_s	96	**39.6**	**441**	39.8	439	39.6	441	96	**39.7**	**441**	39.6	441	39.7	440
649.fotonik3d_s	96	82.4	111	83.3	109	**83.1**	**110**	96	80.8	113	**81.8**	**111**	81.9	111
654.roms_s	96	**55.1**	**286**	54.9	287	56.1	280	96	**56.9**	**277**	53.6	294	57.7	273

SPECspeed®2017_fp_base = 203

SPECspeed®2017_fp_peak = 203

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

```
Stack size set to unlimited using "ulimit -s unlimited"
```

Environment Variables Notes

```
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"
```

General Notes

```
 Binaries compiled on a system with 1x Intel Core i9-799X CPU + 32GB RAM
 memory using Redhat Enterprise Linux 7.5
 Transparent Huge Pages enabled by default
 Prior to runcpu invocation
 Filesystem page cache synced and cleared with:
 sync; echo 3>       /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
```

Platform Notes

```
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

SNC set to Disabled
Patrol Scrub set to Disabled

 Sysinfo program /home/cpu2017/bin/sysinfo
 Rev: r6365 of 2019-08-21 295195f888a3d7edb1e6e46a485a0011
 running on linux-mz3p Sat Nov 30 15:15:31 2019

 SUT (System Under Test) info as seen by some common utilities.
 For more information on this section, see
    https://www.spec.org/cpu2017/Docs/config.html#sysinfo

 From /proc/cpuinfo
    model name : Intel(R) Xeon(R) Platinum 8260L CPU @ 2.40GHz
       4  "physical id"s (chips)
       96 "processors"
    cores, siblings (Caution: counting these is hw and system dependent. The following
    excerpts from /proc/cpuinfo might not be reliable.  Use with caution.)
       cpu cores : 24
       siblings  : 24
       physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
       physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
       physical 2: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
       physical 3: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

 From lscpu:
      Architecture:        x86_64
      CPU op-mode(s):      32-bit, 64-bit
      Byte Order:          Little Endian
      CPU(s):              96
      On-line CPU(s) list: 0-95
      Thread(s) per core:  1
      Core(s) per socket:  24
      Socket(s):           4
      NUMA node(s):        4
      Vendor ID:           GenuineIntel
      CPU family:          6
      Model:               85
      Model name:          Intel(R) Xeon(R) Platinum 8260L CPU @ 2.40GHz
      Stepping:            6
      CPU MHz:             2400.000
      CPU max MHz:         3900.0000
      CPU min MHz:         1000.0000
      BogoMIPS:            4800.00
```

(Continued on next page)

Platform Notes (Continued)

```
      Virtualization:      VT-x
      L1d cache:           32K
      L1i cache:           32K
      L2 cache:            1024K
      L3 cache:            36608K
      NUMA node0 CPU(s):   0-23
      NUMA node1 CPU(s):   24-47
      NUMA node2 CPU(s):   48-71
      NUMA node3 CPU(s):   72-95
      Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
      pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
      lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
      aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
       sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
       tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
      epb cat_l3 cdp_l3 invpcid_single mba tpr_shadow vnmi flexpriority ept vpid fsgsbase
       tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq
       rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec
       xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs stibp
      dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni
       arch_capabilities ssbd

 /proc/cpuinfo cache data
    cache size : 36608 KB

 From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a
 physical chip.
   available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
   node 0 size: 385622 MB
   node 0 free: 385302 MB
   node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
   node 1 size: 387028 MB
   node 1 free: 386852 MB
   node 2 cpus: 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
   node 2 size: 387056 MB
   node 2 free: 386372 MB
   node 3 cpus: 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95
   node 3 size: 387054 MB
   node 3 free: 379920 MB
   node distances:
   node   0   1   2   3
     0:  10  21  21  21
     1:  21  10  21  21
     2:  21  21  10  21
     3:  21  21  21  10
```

(Continued on next page)

Platform Notes (Continued)

```
From /proc/meminfo
   MemTotal:       1583884444 kB
   HugePages_Total:       0
   Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
   os-release:
      NAME="SLES"
      VERSION="15"
      VERSION_ID="15"
      PRETTY_NAME="SUSE Linux Enterprise Server 15"
      ID="sles"
      ID_LIKE="suse"
      ANSI_COLOR="0;32"
      CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
   Linux linux-mz3p 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
   x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault):        No status reported
Microarchitectural Data Sampling:         No status reported
CVE-2017-5754 (Meltdown):                 Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                          via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):        Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):        Mitigation: Indirect Branch Restricted
                                          Speculation, IBPB, IBRS_FW

run-level 3 Nov 30 10:48

SPEC is set to: /home/cpu2017
   Filesystem     Type  Size  Used Avail Use% Mounted on
   /dev/sdb2      xfs   549G   91G  459G  17% /

From /sys/devices/virtual/dmi/id
    BIOS:    Cisco Systems, Inc. C480M5.4.0.3.32.0301190121 03/01/2019
    Vendor:  Cisco
    Product: UCSC-C480-M5
    Serial:  FCH2238W019

Additional information from dmidecode follows.  WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
```

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Platform Notes (Continued)

```
   Memory:
     48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

 (End of data from sysinfo program)
```

Compiler Version Notes

```
==============================================================================
C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)
                | 644.nab_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
                | 654.roms_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
                | 628.pop2_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
  64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
```

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Compiler Version Notes (Continued)

```
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation.  All rights reserved.
------------------------------------------------------------------------------
```

Base Compiler Invocation

C benchmarks:
`icc -m64 -std=c11`

Fortran benchmarks:
`ifort -m64`

Benchmarks using both Fortran and C:
`ifort -m64 icc -m64 -std=c11`

Benchmarks using Fortran, C, and C++:
`icpc -m64 icc -m64 -std=c11 ifort -m64`

Base Portability Flags

603.bwaves_s: `-DSPEC_LP64`
607.cactuBSSN_s: `-DSPEC_LP64`
619.lbm_s: `-DSPEC_LP64`
621.wrf_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian`
627.cam4_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG`
628.pop2_s: `-DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl`
638.imagick_s: `-DSPEC_LP64`
644.nab_s: `-DSPEC_LP64`
649.fotonik3d_s: `-DSPEC_LP64`
654.roms_s: `-DSPEC_LP64`

Base Optimization Flags

C benchmarks:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP`

Fortran benchmarks:
`-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch`

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Base Optimization Flags (Continued)

Fortran benchmarks (continued):
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:

(Continued on next page)

Peak Optimization Flags (Continued)

603.bwaves_s: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-DSPEC_SUPPRESS_OPENMP -DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs`

649.fotonik3d_s: `Same as 603.bwaves_s`

654.roms_s: `-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -nostandard-realloc-lhs`

Benchmarks using both Fortran and C:

621.wrf_s: `-prof-gen`(pass 1) `-prof-use`(pass 2) `-O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`

627.cam4_s: `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`

628.pop2_s: `Same as 621.wrf_s`

Benchmarks using Fortran, C, and C++:
`-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP -nostandard-realloc-lhs`

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.html
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0u1-official-linux64.2019-07-09.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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