Cisco Systems
Cisco UCS B480 M5 (Intel Xeon Gold 6240, 2.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Threads

SPECspeed®2017_fp_base = 184
SPECspeed®2017_fp_peak = Not Run

Hardware
CPU Name: Intel Xeon Gold 6240
Max MHz: 3900
Nominal: 2600
Enabled: 72 cores, 4 chips
Orderable: 2,4 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: default
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SPECspeed®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td>72</td>
<td>66.4</td>
<td>888</td>
<td>66.8</td>
<td>883</td>
<td>67.1</td>
<td>879</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>72</td>
<td>81.1</td>
<td>205</td>
<td>82.3</td>
<td>203</td>
<td>82.0</td>
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<td>619.ibm_s</td>
<td>72</td>
<td>36.6</td>
<td>143</td>
<td>35.2</td>
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<tr>
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<td>140</td>
<td>94.6</td>
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<td>627.cam4_s</td>
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<td>143</td>
<td>61.6</td>
<td>144</td>
<td>61.5</td>
<td>144</td>
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<tr>
<td>628.pop2_s</td>
<td>72</td>
<td>268</td>
<td>44.3</td>
<td>264</td>
<td>44.9</td>
<td>261</td>
<td>45.5</td>
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<tr>
<td>638.imagick_s</td>
<td>72</td>
<td>68.5</td>
<td>211</td>
<td>69.0</td>
<td>209</td>
<td>73.2</td>
<td>197</td>
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<tr>
<td>644.nab_s</td>
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<td>45.8</td>
<td>381</td>
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<td>381</td>
<td>45.8</td>
<td>382</td>
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<tr>
<td>649.fotonik3d_s</td>
<td>72</td>
<td>82.4</td>
<td>111</td>
<td>84.3</td>
<td>108</td>
<td>82.4</td>
<td>111</td>
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<tr>
<td>654.roms_s</td>
<td>72</td>
<td>74.1</td>
<td>212</td>
<td>72.3</td>
<td>218</td>
<td>71.7</td>
<td>220</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
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SPECspeed®2017_fp_base = 184
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Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edble6e46a485a0011
running on linux-db10 Mon Nov 4 11:46:00 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
4 "physical id"s (chips)
72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 2: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 3: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240 CPU @ 2.60GHz
Stepping: 6
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00

(Continued on next page)
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SPECspeed®2017_fp_peak = Not Run

CPU2017 License:
Test Date: Nov-2019
Hardware Availability: Apr-2019
Softwer Availability: May-2019

Platform Notes (Continued)

<table>
<thead>
<tr>
<th>Virtualization:</th>
<th>VT-x</th>
</tr>
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<tbody>
<tr>
<td>L1d cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L1i cache:</td>
<td>32K</td>
</tr>
<tr>
<td>L2 cache:</td>
<td>1024K</td>
</tr>
<tr>
<td>L3 cache:</td>
<td>25344K</td>
</tr>
<tr>
<td>NUMA node0 CPU(s):</td>
<td>0-17</td>
</tr>
<tr>
<td>NUMA node1 CPU(s):</td>
<td>18-35</td>
</tr>
<tr>
<td>NUMA node2 CPU(s):</td>
<td>36-53</td>
</tr>
<tr>
<td>NUMA node3 CPU(s):</td>
<td>54-71</td>
</tr>
</tbody>
</table>

Flags:
- fpu
- vme
- de
- pse
- sep
- mtrr
- pae
- mce
- cx8
- apic
- sep
- mtrr
- pae
- mce
- cx8
- apic

Platform Notes (Continued)

From numactl --hardware

WARNING: a numactl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 385627 MB
node 0 free: 384489 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 387029 MB
node 1 free: 383687 MB
node 2 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
node 2 size: 387058 MB
node 2 free: 386815 MB
node 3 cpus: 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 3 size: 387055 MB
node 3 free: 386710 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

(Continued on next page)
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Test Date: Nov-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

From /proc/meminfo
MemTotal: 1583892160 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-db10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): No status reported
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Nov 4 09:29

SPEC is set to: /home/cpu2017

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. B480M5.4.0.4b.0.0407190454 04/07/2019
Vendor: Cisco Systems Inc
Product: UCSB-B480-M5
Serial: FLM225202G1

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
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SPEC®2017_FP_peak = Not Run

CPU2017 License: 9019
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Tested by: Cisco Systems

Platform Notes (Continued)

Memory:
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)</th>
</tr>
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<tbody>
<tr>
<td>Intel(R) C</td>
<td>Intel(R) 64 Compiler for applications running on Intel(R) 64,</td>
</tr>
<tr>
<td></td>
<td>Version 19.0.4.227 Build 20190416</td>
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<td></td>
<td>Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>-----------------</td>
<td>-----------------------------------------------------</td>
</tr>
<tr>
<td>Intel(R) C, Fortran</td>
<td>607.cactuBSSN_s(base)</td>
</tr>
<tr>
<td>-------------------</td>
<td>---------------------------------------------------</td>
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<td>-----------------</td>
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<td>Fortran</td>
<td>603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)</td>
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<td>-----------------</td>
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<tr>
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<td></td>
<td>64, Version 19.0.4.227 Build 20190416</td>
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<td>621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)</td>
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Compiler Version Notes (Continued)

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

(Continued on next page)
SPEC CPU®2017 Floating Point Speed Result

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Hardware Availability: Apr-2019
Software Availability: May-2019

Base Optimization Flags (Continued)

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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