Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5218B, 2.30GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>179</th>
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</thead>
<tbody>
<tr>
<td>SPECrate®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Date:** Oct-2019  
**Hardware Availability:** Apr-2019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Software Availability:** May-2019

<table>
<thead>
<tr>
<th>Copies</th>
<th>0</th>
<th>20</th>
<th>40</th>
<th>60</th>
<th>80</th>
<th>100</th>
<th>120</th>
<th>140</th>
<th>160</th>
<th>180</th>
<th>200</th>
<th>220</th>
<th>240</th>
<th>260</th>
<th>280</th>
<th>300</th>
<th>320</th>
<th>340</th>
<th>360</th>
<th>380</th>
<th>400</th>
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<th>460</th>
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</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>64</td>
<td>64</td>
<td>64</td>
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<td>64</td>
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<tr>
<td>507.cactuBSSN_r</td>
<td>64</td>
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<tr>
<td>508.namd_r</td>
<td>64</td>
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<tr>
<td>510.parest_r</td>
<td>64</td>
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<td>511.povray_r</td>
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<td>519.lhm_r</td>
<td>64</td>
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<td>521.wrf_r</td>
<td>64</td>
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<td>526.blender_r</td>
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</tr>
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<td>527.cam4_r</td>
<td>64</td>
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</tr>
<tr>
<td>538.imagick_r</td>
<td>64</td>
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<td>64</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>64</td>
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<tr>
<td>549.fotonik3d_r</td>
<td>64</td>
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</tr>
<tr>
<td>554.roms_r</td>
<td>64</td>
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</tr>
</tbody>
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**Hardware**
- **CPU Name:** Intel Xeon Gold 5218B
- **Max MHz:** 3900
- **Nominal:** 2300
- **Enabled:** 32 cores, 2 chips, 2 threads/core
- **Orderable:** 1,2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 22 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2666)
- **Storage:** 1 x 240 GB M.2 SATA SSD
- **Other:** None

**Software**
- **OS:** SUSE Linux Enterprise Server 15 4.12.14-23-default
- **Compiler:** C/C++; Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** btrfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** Not Applicable
- **Other:** None
- **Power Management:** default
## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Gold 5218B, 2.30GHz)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>64</td>
<td>1367</td>
<td></td>
<td>1367</td>
<td></td>
<td>1368</td>
<td></td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>64</td>
<td>560</td>
<td>145</td>
<td>559</td>
<td>145</td>
<td>559</td>
<td>145</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>64</td>
<td>448</td>
<td>136</td>
<td>449</td>
<td>135</td>
<td>451</td>
<td>135</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>64</td>
<td>1547</td>
<td>108</td>
<td>1563</td>
<td>107</td>
<td>1558</td>
<td>107</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>64</td>
<td>742</td>
<td>201</td>
<td>739</td>
<td>202</td>
<td>741</td>
<td>202</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>64</td>
<td>629</td>
<td>107</td>
<td>629</td>
<td>107</td>
<td>629</td>
<td>107</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>64</td>
<td>732</td>
<td>196</td>
<td>719</td>
<td>199</td>
<td>718</td>
<td>200</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>64</td>
<td>573</td>
<td>170</td>
<td>575</td>
<td>170</td>
<td>573</td>
<td>170</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>64</td>
<td>589</td>
<td>190</td>
<td>579</td>
<td>193</td>
<td>580</td>
<td>193</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>64</td>
<td>419</td>
<td>380</td>
<td>420</td>
<td>379</td>
<td>421</td>
<td>378</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>64</td>
<td>375</td>
<td>288</td>
<td>376</td>
<td>286</td>
<td>374</td>
<td>288</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>64</td>
<td>1718</td>
<td>145</td>
<td>1718</td>
<td>145</td>
<td>1718</td>
<td>145</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>64</td>
<td>1155</td>
<td>88.0</td>
<td>1152</td>
<td>88.3</td>
<td>1153</td>
<td>88.2</td>
</tr>
</tbody>
</table>

### Results Table

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### Environment Variables Notes

Environment variables set by runcpu before the start of the run:

```
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
```

### General Notes

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5218B, 2.30GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 179
SPECrate®2017_fp_peak = Not Run

General Notes (Continued)

runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5755 (Spectre variant 2)
is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195ff888a3d7ed61e6e46a485a0011
running on linux-cud8 Sat Oct 19 00:34:59 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4

(Continued on next page)
## SPEC CPU®2017 Floating Point Rate Result

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Gold 5218B, 2.30GHz)  

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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Oct-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

```
Vendor ID:           GenuineIntel  
CPU family:          6  
Model:               85  
Model name:          Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz  
Stepping:            6  
CPU MHz:             2300.000  
CPU max MHz:         3900.0000  
CPU min MHz:         1000.0000  
BogoMIPS:            4600.00  
Virtualization:      VT-x  
L1d cache:           32K  
L1i cache:           32K  
L2 cache:            1024K  
L3 cache:            22528K  
NUMA node0 CPU(s):   0-3,8-11,32-35,40-43  
NUMA node1 CPU(s):   4-7,12-15,36-39,44-47  
NUMA node2 CPU(s):   16-19,24-27,48-51,56-59  
NUMA node3 CPU(s):   20-23,28-31,52-55,60-63  
Flags:               fpu vme de pse mce pmx cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperff perf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pinn mba tpr_shadow vmx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rt_rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsave x savec xgetbv xsaves cqm_llc cqm_occup_llc cqm_mbb total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd
```

From numactl --hardware  
```
WARNING: a numactl 'node' might or might not correspond to a physical chip.  
available: 4 nodes (0-3)  
node 0 cpus: 0 1 2 3 8 9 10 11 12 32 33 34 35 36 40 41 42 43  
node 0 size: 192074 MB  
node 0 free: 186248 MB  
node 1 cpus: 4 5 6 7 12 13 14 15 36 37 38 39 44 45 46 47  
node 1 size: 193527 MB  
node 1 free: 189830 MB  
node 2 cpus: 16 17 18 19 24 25 26 27 48 49 50 51 56 57 58 59  
node 2 size: 193527 MB  
node 2 free: 189848 MB  
node 3 cpus: 20 21 22 23 28 29 30 31 52 53 54 55 60 61 62 63
```
Platform Notes (Continued)

node 3 size: 193526 MB
node 3 free: 189868 MB
node distances:
  node 0 1 2 3
  0: 10 11 21 21
  1: 11 10 21 21
  2: 21 21 10 11
  3: 21 21 11 10

From /proc/meminfo
  MemTotal:       791200136 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-cud8 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault):        No status reported
Microarchitectural Data Sampling:           No status reported
CVE-2017-5754 (Meltdown):                 Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled
                                          via prctl and seccomp
CVE-2017-5753 (Spectre variant 1):        Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2):        Mitigation: Indirect Branch Restricted
                                          Speculation, IBPB, IBRS_FW

run-level 3 Oct 18 19:27

SPEC is set to: /home/cpu2017
  Filesystem Type    Size  Used Avail Use% Mounted on
  /dev/sda2 btrfs 224G 52G 172G 24%  /home

From /sys/devices/virtual/dmi/id
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5218B, 2.30GHz)

SPECrate®2017_fp_base = 179
SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

BIOS: Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
Vendor: Cisco Systems Inc
Product: UCSC-C220-M5SX
Serial: WZP22380CRE

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
Memory: 24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)
The marketing name for the processor in this result, which appears in the CPU name and hardware model areas, is different from sysinfo because a pre-production processor was used. The pre-production processor differs from the production processor in name only.

Compiler Version Notes

C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
-----------------|---------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------|---------------------------------------------------------

C++            | 508.namd_r(base) 510.parest_r(base)
-----------------|---------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------|---------------------------------------------------------

C++, C         | 511.povray_r(base) 526.blender_r(base)
-----------------|---------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------|---------------------------------------------------------

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5218B, 2.30GHz)

SPECrates:
- SPECrate®2017_fp_base = 179
- SPECrate®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

C++, C, Fortran | 507.cactuBSSN\_r(base)

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran | 503.bwaves\_r(base) 549.fotonik3d\_r(base) 554.roms\_r(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran, C | 521.wrf\_r(base) 527.cam4\_r(base)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
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Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5218B, 2.30GHz)

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>Cisco Systems</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date</td>
<td>Oct-2019</td>
</tr>
<tr>
<td>Hardware Availability</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

SPECrate®2017_fp_base = 179
SPECrate®2017_fp_peak = Not Run

**Base Compiler Invocation (Continued)**

Benchmarks using both C and C++:
```
icpc -m64 icc -m64 -std=c11
```
Benchmarks using Fortran, C, and C++:
```
icpc -m64 icc -m64 -std=c11 ifort -m64
```

**Base Portability Flags**

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -funsigned-char
527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

**Base Optimization Flags**

C benchmarks:
```
xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

C++ benchmarks:
```
xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4
```

Fortran benchmarks:
```
xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte
```

Benchmarks using both Fortran and C:
```
xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
```

(Continued on next page)
## Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Gold 5218B, 2.30GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

### SPECrate®2017_fp_base = 179
### SPECrate®2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>Test Date:</th>
<th>Oct-2019</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
<tr>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### Base Optimization Flags (Continued)

**Benchmarks using both Fortran and C (continued):**
- `n ostandard-realloc-lhs -align array32byte`

**Benchmarks using both C and C++:**
- `xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch`
- `ffinite-math-only -gopt-mem-layout-trans=4`

**Benchmarks using Fortran, C, and C++:**
- `xCORE-AVX512 -ipo -O3 -no-prec-div -gopt-prefetch`
- `ffinite-math-only -gopt-mem-layout-trans=4 -auto`
- `n ostandard-realloc-lhs -align array32byte`

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links: