Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 6254, 3.10GHz)

**SPECspeed®2017_int_base = 10.4**

**SPECspeed®2017_int_peak = 10.6**

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<tr>
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<th>SPECspeed®2017_int_peak (10.6)</th>
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<td>600.perlbench_s 72</td>
<td>6.94 8.15 9.95</td>
<td>10.2 12.8 12.9</td>
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<td>8.2 8.5</td>
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<tr>
<td>623.xalancbmk_s 72</td>
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<td>625.x264_s 72</td>
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<tr>
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<td>641.leela_s 72</td>
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<td>648.exchange2_s 72</td>
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**CPU2017 License:** 9019  
**Test Date:** Oct-2019  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Apr-2019  
**Tested by:** Cisco Systems  
**Software Availability:** May-2019

**Hardware**

- **CPU Name:** Intel Xeon Gold 6254
- **Max MHz:** 4000
- **Nominal:** 3100
- **Enabled:** 72 cores, 4 chips
- **Orderable:** 2.4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 24.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

**Software**

- **OS:** SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-25.28-default
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** default
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6254, 3.10GHz)

Results Table

<table>
<thead>
<tr>
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<th>Seconds</th>
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</tbody>
</table>

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.6

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

Environment Variables Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

General Notes
Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
SPEC CPU®2017 Integer Speed Result

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6254, 3.10GHz)

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.6

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r6365 of 2019-08-21 295195f888a3d7edbc6e46a485a0011
running on linux-75co Thu Oct 10 09:55:53 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6254 CPU @ 3.10GHz
  4 "physical id"s (chips)
  72 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 2: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 3: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 72
On-line CPU(s) list: 0-71
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6254 CPU @ 3.10GHz
Stepping: 6
CPU MHz: 3100.000
CPU max MHz: 4000.0000
CPU min MHz: 1200.0000
BogoMIPS: 6200.00

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6254, 3.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.6

Platform Notes (Continued)

Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-17
NUMA node1 CPU(s): 18-35
NUMA node2 CPU(s): 36-53
NUMA node3 CPU(s): 54-71
Flags: fpu vme de pse tsc msr pae mce cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpmr pdm cmid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_ppm ssbd mba ibrs ibpb ibrs_enabled tpr_shadow vmi intel_pmu flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 3dnow invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsavesopt xsaveopt xsaves cgx_saveopt xsavec xgetbv1 xsaveopt cqm_llc cqm_occup_llc cqm_mbb cqm_mbb_local dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni flush_l1d arch_capabilities

From numacl --hardware WARNING: a numacl 'node' might or might not correspond to a physical chip.

available: 4 nodes (0-3)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
node 0 size: 385637 MB
node 0 free: 384935 MB
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
node 1 size: 387068 MB
node 1 free: 386812 MB
node 2 cpus: 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
node 2 size: 387039 MB
node 2 free: 386832 MB
node 3 cpus: 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71
node 3 size: 387066 MB
node 3 free: 386861 MB
node distances:
node 0 1 2 3
0: 10 21 21 21
1: 21 10 21 21
2: 21 21 10 21
3: 21 21 21 10

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6254, 3.10GHz)

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.6

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

From /proc/meminfo
MemTotal: 1583934724 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-75co 4.12.14-25.28-default #1 SMP Wed Jan 16 20:00:47 UTC 2019 (dd6077c)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2018-3620 (L1 Terminal Fault): Not affected
Microarchitectural Data Sampling: No status reported
CVE-2017-5754 (Meltdown): Not affected
CVE-2018-3639 (Speculative Store Bypass): Mitigation: Speculative Store Bypass disabled via prctl and seccomp
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Enhanced IBRS, IBPB: conditional, RSB filling

run-level 3 Oct 10 09:47

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda3 xfs 177G 69G 109G 39% /home

From /sys/devices/virtual/dmi/id
BIOS: Cisco Systems, Inc. C480M5.4.0.4g.0.0712190013 07/12/2019
Vendor: Cisco Systems Inc
Product: UCSC-C480-M5
Serial: FCH2223W00A

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

(Continued on next page)
## SPEC CPU®2017 Integer Speed Result

**Cisco Systems**  
Cisco UCS C480 M5 (Intel Xeon Gold 6254, 3.10GHz)  

<table>
<thead>
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<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
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<td>10.4</td>
<td>10.6</td>
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**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Oct-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Platform Notes (Continued)

Memory:  
48x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

### Compiler Version Notes

```
<table>
<thead>
<tr>
<th>Language</th>
<th>Benchmark(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)</td>
</tr>
</tbody>
</table>
|          | Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
|          | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| C++      | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak) |
|          | Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
|          | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
| Fortran  | 648.exchange2_s(base, peak) |
|          | Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
|          | Copyright (C) 1985-2019 Intel Corporation. All rights reserved. |
```

### Base Compiler Invocation

**C benchmarks:**  
`icc -m64 -std=c11`

**C++ benchmarks:**  
`icpc -m64`

**Fortran benchmarks:**  
`ifort -m64`
## Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6254, 3.10GHz)  

| SPECspeed®2017_int_base |= 10.4 |
| SPECspeed®2017_int_peak |= 10.6 |

### CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems  
Test Date: Oct-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

### Base Portability Flags
- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64  
- 602.gcc_s: -DSPEC_LP64  
- 605.mcf_s: -DSPEC_LP64  
- 620.omnetpp_s: -DSPEC_LP64  
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX  
- 625.x264_s: -DSPEC_LP64  
- 631.deepsjeng_s: -DSPEC_LP64  
- 641.leela_s: -DSPEC_LP64  
- 648.exchange2_s: -DSPEC_LP64  
- 657.xz_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**  
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
- -L/usr/local/je5.0.1-64/lib -ljemalloc

**C++ benchmarks:**  
- -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
- -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc

**Fortran benchmarks:**  
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
- -nostandard-realloc-lhs

### Peak Compiler Invocation

**C benchmarks:**  
- icc -m64 -std=c11

**C++ benchmarks:**  
- icpc -m64

**Fortran benchmarks:**  
- ifort -m64
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 6254, 3.10GHz)

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.6

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Oct-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Portability Flags
Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:

600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/je5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

(Continued on next page)
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SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = 10.6

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Peak Optimization Flags (Continued)

631.deepsjeng_s: Same as 623.xalancbmk_s
641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

Originally published on 2019-11-04.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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