## Cisco Systems

Cisco UCS C220 M5 (Intel Xeon Bronze 3204, 1.90GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 40.7</th>
<th>SPECrate®2017_int_peak = 41.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU2017 License: 9019</td>
<td>Test Date: Sep-2019</td>
</tr>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

### Hardware

- **CPU Name:** Intel Xeon Bronze 3204
- **Max MHz:** 1900
- **Nominal:** 1900
- **Enabled:** 12 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 8.25 MB I+D on chip per chip
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2133)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** No
- **Firmware:** Version 4.0.4g released Jul-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --

### SPEC CPU®2017 Integer Rate Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench</td>
<td>12</td>
<td>38.4</td>
<td>32.7</td>
</tr>
<tr>
<td>gcc</td>
<td>12</td>
<td>40.4</td>
<td>38.4</td>
</tr>
<tr>
<td>mcf</td>
<td>12</td>
<td>50.7</td>
<td>50.6</td>
</tr>
<tr>
<td>omnetpp</td>
<td>12</td>
<td>30.3</td>
<td>30.3</td>
</tr>
<tr>
<td>xalancbmk</td>
<td>12</td>
<td>48.1</td>
<td></td>
</tr>
<tr>
<td>x264</td>
<td>12</td>
<td></td>
<td>70.8</td>
</tr>
<tr>
<td>deepsjeng</td>
<td>12</td>
<td>32.7</td>
<td>34.6</td>
</tr>
<tr>
<td>leela</td>
<td>12</td>
<td>27.0</td>
<td>27.0</td>
</tr>
<tr>
<td>exchange2</td>
<td>12</td>
<td></td>
<td>85.7</td>
</tr>
<tr>
<td>xz</td>
<td>12</td>
<td>24.0</td>
<td>24.0</td>
</tr>
</tbody>
</table>

**Copies**

<table>
<thead>
<tr>
<th>SPECrate®2017_int (40.7)</th>
<th>SPECrate®2017_int_peak (41.6)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
RESULTS Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>12</td>
<td>584</td>
<td>32.7</td>
<td>585</td>
<td>32.7</td>
<td>584</td>
<td>32.7</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>12</td>
<td>442</td>
<td>38.4</td>
<td>443</td>
<td>38.4</td>
<td>442</td>
<td>38.5</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>12</td>
<td>383</td>
<td>50.7</td>
<td>383</td>
<td>50.7</td>
<td>383</td>
<td>50.6</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>12</td>
<td>519</td>
<td>30.3</td>
<td>520</td>
<td>30.3</td>
<td>520</td>
<td><strong>30.3</strong></td>
</tr>
<tr>
<td>523.xalanbmk_r</td>
<td>12</td>
<td>252</td>
<td>50.2</td>
<td><strong>252</strong></td>
<td>50.3</td>
<td>251</td>
<td>50.4</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>12</td>
<td>297</td>
<td>70.8</td>
<td>297</td>
<td><strong>70.8</strong></td>
<td>297</td>
<td>70.8</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>12</td>
<td>421</td>
<td>32.7</td>
<td><strong>421</strong></td>
<td><strong>32.7</strong></td>
<td>421</td>
<td>32.7</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>12</td>
<td>735</td>
<td><strong>27.0</strong></td>
<td>735</td>
<td>27.1</td>
<td>735</td>
<td>27.0</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>12</td>
<td>367</td>
<td>85.7</td>
<td>367</td>
<td>85.7</td>
<td><strong>367</strong></td>
<td><strong>85.7</strong></td>
</tr>
<tr>
<td>557.xz_r</td>
<td>12</td>
<td>540</td>
<td>24.0</td>
<td><strong>540</strong></td>
<td><strong>24.0</strong></td>
<td>540</td>
<td>24.0</td>
</tr>
</tbody>
</table>

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3204, 1.90GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_int_base = 40.7
SPECrate®2017_int_peak = 41.6

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Settings:
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-3yo3 Mon Sep 23 14:33:42 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Bronze 3204 CPU @ 1.90GHz
  2 "physical id"s (chips)
  12 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 6
  siblings : 6
  physical 0: cores 0 1 2 3 4 5
  physical 1: cores 0 1 2 3 4 5

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 12
On-line CPU(s) list: 0-11
Thread(s) per core: 1
Core(s) per socket: 6
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Bronze 3204 CPU @ 1.90GHz
Stepping: 6

(Continued on next page)
## SPEC CPU®2017 Integer Rate Result

**Cisco Systems**  
Cisco UCS C220 M5 (Intel Xeon Bronze 3204, 1.90GHz)  

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Sep-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

### SPECrate®2017_int_base = 40.7  
### SPECrate®2017_int_peak = 41.6

## Platform Notes (Continued)

- **CPU MHz:** 1900.000  
- **CPU max MHz:** 1900.0000  
- **CPU min MHz:** 800.0000  
- **BogoMIPS:** 3800.00  
- **Virtualization:** VT-x  
- **L1d cache:** 32K  
- **L1i cache:** 32K  
- **L2 cache:** 1024K  
- **L3 cache:** 8448K  
- **NUMA node0 CPU(s):** 0-5  
- **NUMA node1 CPU(s):** 6-11  
- **Flags:** fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_puin mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2  
- **cpu architect:**  
- **flags:**  
- **cpu capabilities:**  
- **cpu features:**  
- **cpu info:**  
- **cpu info cache data:**  
- **cache size:** 8448 KB

From `numactl --hardware`  
**WARNING:** a numactl 'node' might or might not correspond to a physical chip.  
- **available:** 2 nodes (0-1)  
- **node 0 cpus:** 0 1 2 3 4 5  
- **node 0 size:** 385636 MB  
- **node 0 free:** 385133 MB  
- **node 1 cpus:** 6 7 8 9 10 11  
- **node 1 size:** 387029 MB  
- **node 1 free:** 386591 MB  
- **node distances:**  
- **node 0:** 0 1  
- **node 1:** 10 21  
- **node 0:** 1 21  
- **node 1:** 10  

From `/proc/meminfo`  
**MemTotal:** 791210432 KB  
**HugePages_Total:** 0  
**Hugepagesize:** 2048 KB  

From `/etc/*release* /etc/*version*  
(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3204, 1.90GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 40.7</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak = 41.6</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019  Test Date: Sep-2019
Test Sponsor: Cisco Systems  Hardware Availability: Apr-2019
Tested by: Cisco Systems  Software Availability: May-2019

---

### Platform Notes (Continued)

```bash
os-release:
  NAME="SLES"
  VERSION="15"
  VERSION_ID="15"
  PRETTY_NAME="SUSE Linux Enterprise Server 15"
  ID="sles"
  ID_LIKE="suse"
  ANSI_COLOR="0;32"
  CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-3yo3 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 23 14:26

SPEC is set to: /home/cpu2017
  Filesystem     Type  Size  Used Avail Use% Mounted on
  /dev/sda1      xfs   224G   20G  204G   9% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- BIOS Cisco Systems, Inc. C220M5.4.0.4g.0.0712190011 07/12/2019
- Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2133

(End of data from sysinfo program)
```

---

### Compiler Version Notes

```
C       | 502.gcc_r(peak)
--------|----------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3204, 1.90GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 40.7
SPECrate®2017_int_peak = 41.6

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

==============================================================================
C      | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
C      | 502.gcc_r(peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
C      | 500.perlbench_r(base, peak) 502.gcc_r(base) 505.mcf_r(base, peak)
| 525.x264_r(base, peak) 557.xz_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
C++     | 523.xalancbmk_r(peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version
19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
C++     | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base)
| 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

(Continued on next page)
Cisco Systems  
Cisco UCS C220 M5 (Intel Xeon Bronze 3204, 1.90GHz)  

SPECrate®2017_int_base = 40.7  
SPECrate®2017_int_peak = 41.6

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Sep-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Compiler Version Notes (Continued)

Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

C++ | 520.omnetpp_r(base, peak) 523.xalancbmk_r(base) 531.deepsjeng_r(base, peak) 541.leela_r(base, peak)  

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Fortran | 548.exchange2_r(base, peak)  

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:  
icc -m64 -std=c11

C++ benchmarks:  
icpc -m64

Fortran benchmarks:  
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64  
502.gcc_r: -DSPEC_LP64  
505.mcf_r: -DSPEC_LP64  
520.omnetpp_r: -DSPEC_LP64  
523.xalancbmk_r: -DSPEC_LP64 -DSPEC_LINUX  
525.x264_r: -DSPEC_LP64  
531.deepsjeng_r: -DSPEC_LP64  
541.leela_r: -DSPEC_LP64

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3204, 1.90GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
SPECrate®2017_int_base = 40.7
SPECrate®2017_int_peak = 41.6

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Base Portability Flags (Continued)

548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-lhs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

Peak Compiler Invocation

C benchmarks (except as noted below):
icc -m64 -std=c11

502.gcc_r icc -m32 -std=c11 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

C++ benchmarks (except as noted below):
icpc -m64

523.xalancbmk_r icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3204, 1.90GHz)

SPECrates:
SPECrates\textsuperscript{2017\_int\_base} = 40.7
SPECrates\textsuperscript{2017\_int\_peak} = 41.6

CPU\textsuperscript{2017\_License}: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Portability Flags

500.perlbench\_r: -DSPEC\_LP64 -DSPEC\_LINUX\_X64
502.gcc\_r: -D\_FILE\_OFFSET\_BITS=64
505.mcf\_r: -DSPEC\_LP64
520.omnetpp\_r: -DSPEC\_LP64
523.xalancbmk\_r: -D\_FILE\_OFFSET\_BITS=64 -DSPEC\_LINUX
525.x264\_r: -DSPEC\_LP64
531.deepsjeng\_r: -DSPEC\_LP64
541.leela\_r: -DSPEC\_LP64
548.exchange2\_r: -DSPEC\_LP64
557.xz\_r: -DSPEC\_LP64

Peak Optimization Flags

C benchmarks:

500.perlbench\_r: -Wl,-z,muldefs -prof-use(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-fno-strict-overflow
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

502.gcc\_r: -Wl,-z,muldefs -prof-use(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

505.mcf\_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

525.x264\_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-fno-alias
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

557.xz\_r: Same as 505.mcf\_r

C++ benchmarks:

520.omnetpp\_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

(Continued on next page)
Cisco Systems
Cisco UCS C220 M5 (Intel Xeon Bronze 3204, 1.90GHz)

SPECrate®2017_int_base = 40.7
SPECrate®2017_int_peak = 41.6

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Sep-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Peak Optimization Flags (Continued)

523.xalancbmk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-L/usr/local/je5.0.1-32/lib -ljemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -nostandard-realloc-1hs -align array32byte
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revJ.xml

SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-23 05:03:41-0400.
Originally published on 2019-11-04.