# SPEC CPU®2017 Integer Speed Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Silver 4215, 2.50GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.63</td>
<td>8.80</td>
</tr>
</tbody>
</table>

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)
- **Compiler:** C/C++: Version 19.0.4.227 of Intel C/C++, Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 4.0.4d released May-2019
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --

### Hardware

- **CPU Name:** Intel Xeon Silver 4215
- **Max MHz:** 3500
- **Nominal:** 2500
- **Enabled:** 16 cores, 2 chips
- **Orderable:** 2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 2 MB I+D on chip per core
- **L3:** 11 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R, running at 2400)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None

### Test Details

- **CPU2017 License:** 9019
- **Test Sponsor:** Cisco Systems
- **Tested by:** Cisco Systems
- **Test Date:** Sep-2019
- **Hardware Availability:** Apr-2019
- **Software Availability:** May-2019

<table>
<thead>
<tr>
<th>Thread</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>5.96</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>8.07</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>11.4</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>5.20</td>
</tr>
<tr>
<td>623.xalancbmk_s</td>
<td>11.1</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>12.4</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>5.01</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>4.28</td>
</tr>
<tr>
<td>648.exchange2_s</td>
<td>15.0</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>18.2</td>
</tr>
</tbody>
</table>

**Threads:**

- **600.perlbench_s:** 16
- **602.gcc_s:** 16
- **605.mcf_s:** 16
- **620.omnetpp_s:** 16
- **623.xalancbmk_s:** 16
- **625.x264_s:** 16
- **631.deepsjeng_s:** 16
- **641.leela_s:** 16
- **648.exchange2_s:** 16
- **657.xz_s:** 16

**SPECspeed®2017_int_base (8.63)**

**SPECspeed®2017_int_peak (8.80)**
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215, 2.50GHz)

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>16</td>
<td>299</td>
<td>5.94</td>
<td>297</td>
<td>5.98</td>
<td>298</td>
<td>5.96</td>
<td>16</td>
<td>259</td>
<td>6.85</td>
<td>259</td>
<td>6.86</td>
<td>259</td>
<td>6.85</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>16</td>
<td>496</td>
<td>8.04</td>
<td>492</td>
<td>8.09</td>
<td>493</td>
<td>8.07</td>
<td>16</td>
<td>483</td>
<td>8.24</td>
<td>479</td>
<td>8.31</td>
<td>481</td>
<td>8.29</td>
</tr>
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<td>16</td>
<td>414</td>
<td>11.4</td>
<td>412</td>
<td>11.4</td>
<td>413</td>
<td>11.4</td>
<td>16</td>
<td>409</td>
<td>11.5</td>
<td>411</td>
<td>11.5</td>
<td>416</td>
<td>11.4</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>16</td>
<td>314</td>
<td>5.20</td>
<td>312</td>
<td>5.22</td>
<td>314</td>
<td>5.19</td>
<td>16</td>
<td>311</td>
<td>5.24</td>
<td>312</td>
<td>5.23</td>
<td>311</td>
<td>5.25</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>16</td>
<td>128</td>
<td>11.1</td>
<td>128</td>
<td>11.1</td>
<td>129</td>
<td>11.0</td>
<td>16</td>
<td>129</td>
<td>11.0</td>
<td>128</td>
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</tr>
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<td>5.01</td>
<td>286</td>
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<td>286</td>
<td>5.01</td>
<td>16</td>
<td>286</td>
<td>5.00</td>
<td>286</td>
<td>5.00</td>
<td>286</td>
<td>5.00</td>
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<td>16</td>
<td>398</td>
<td>4.29</td>
<td>399</td>
<td>4.28</td>
<td>398</td>
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<td>16</td>
<td>398</td>
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<td>340</td>
<td>18.2</td>
<td>339</td>
<td>18.2</td>
<td>16</td>
<td>335</td>
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SPECspeed®2017_int_base = 8.63
SPECspeed®2017_int_peak = 8.80

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
  sync; echo 3>&1 > /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215, 2.50GHz)

SPECspeed®2017_int_base = 8.63
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-uuav Tue Sep  3 14:19:35 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
 model name : Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
 2 "physical id"s (chips)
 16 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
 cpu cores : 8
siblings : 8
physical 0: cores 0 1 2 3 4 5 6 7
physical 1: cores 0 1 2 3 4 5 6 7

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 16
On-line CPU(s) list: 0-15
Thread(s) per core: 1
Core(s) per socket: 8
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Silver 4215 CPU @ 2.50GHz
Stepping: 6
CPU MHz: 2500.000
CPU max MHz: 3500.0000
CPU min MHz: 1000.0000
BogoMIPS: 5000.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K

(Continued on next page)
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### CPU2017 License:
9019

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<tr>
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<td>May-2019</td>
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</tr>
</tbody>
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## Platform Notes (Continued)

- **L2 cache:** 1024K
- **L3 cache:** 11264K
- **NUMA node0 CPU(s):** 0-7
- **NUMA node1 CPU(s):** 8-15
- **Flags:** fpu vme de pse tsc msr pae mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcdt dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_13 cdp_13 invpcid_single intel_patin mba tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsavec xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local ibpb ibrs ibt dbcriden ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pkp ospke avx512_vnni arch_capabilities ssbd

From `numactl --hardware`

```
WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7
node 0 size: 385606 MB
node 0 free: 385049 MB
node 1 cpus: 8 9 10 11 12 13 14 15
node 1 size: 387058 MB
node 1 free: 386613 MB
node distances:
  node 0: 10 21
  node 1: 21 10
```

From `/proc/meminfo`

```
MemTotal: 791209204 kB
MemAvailable: 385049 MB
MemFree: 386613 MB
MemCpus: 10 21
```

From `/etc/*release*`

```
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
```

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215, 2.50GHz)

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Tested by: Cisco Systems

Test Date: Sep-2019  
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Platform Notes (Continued)

ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:  
Linux linux-uuav 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)  
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected  
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization  
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Sep 3 13:53

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda1      xfs   224G   20G  204G   9% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================  
C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)  
==============================================================================  
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.4.227 Build 20190416  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================  

C++     | 620.omnetpp_s(base, peak) 623.xalanchmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)  
==============================================================================  
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Silver 4215, 2.50GHz)

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Test Date: Sep-2019
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Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

-----------------------------------------------------------------------------------

Fortran | 648.exchange2_s(base, peak)
-----------------------------------------------------------------------------------

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
-----------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

(Continued on next page)
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### Base Optimization Flags (Continued)

**C benchmarks (continued):**
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

**C++ benchmarks:**
- `-Wl,-z,muldef -xCORE-AVX512 -ipo -O3 -no-prec-div`
- `-qopt-mem-layout-trans=4`
- `-L/usr/local/IntelCompiler19 compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc`

**Fortran benchmarks:**
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4 -nostandard-realloc-lhs`

### Peak Compiler Invocation

**C benchmarks:**
- `icc -m64 -std=c11`

**C++ benchmarks:**
- `icpc -m64`

**Fortran benchmarks:**
- `ifort -m64`

### Peak Portability Flags

Same as Base Portability Flags

### Peak Optimization Flags

**C benchmarks:**
- `600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`
- `-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3`
- `-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp`
- `-DSPEC_OPENMP -fno-strict-overflow`
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

- `602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`
- `-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3`

(Continued on next page)
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Peak Optimization Flags (Continued)

602.gcc_s (continued):
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.5 on 2019-09-03 04:49:34-0400.  
Originally published on 2019-10-01.