Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6246, 3.30GHz)

| Test Sponsor: | Cisco Systems | Test Date: | Aug-2019 |
| Test Date: | Aug-2019 | Hardware Availability: | Apr-2019 |
| Tested by: | Cisco Systems | Software Availability: | May-2019 |
| CPU2017 License: | 9019 | |
| SPECspeed®2017_int_base = 10.2 |
| SPECspeed®2017_int_peak = 10.4 |

### Hardware

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<tr>
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<th>SPECspeed®2017_int_peak (10.4)</th>
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<td>605.mcf_s 24</td>
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<td>620.omnetpp_s 24</td>
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<tr>
<td>623.xalancbmk_s 24</td>
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<td>625.x264_s 24</td>
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<td>641.leela_s 24</td>
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<td>648.exchange2_s 24</td>
<td>18.0</td>
<td>18.0</td>
</tr>
<tr>
<td>657.xz_s 24</td>
<td>21.0</td>
<td>21.1</td>
</tr>
</tbody>
</table>

### Software

| OS: | SUSE Linux Enterprise Server 15 (x86_64) |
| compiler: | C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux |
| Parallel: | Yes |
| Firmware: | Version 4.0.3 released Mar-2019 |
| File System: | xfs |
| System State: | Run level 3 (multi-user) |
| Base Pointers: | 64-bit |
| Peak Pointers: | 64-bit |
| Other: | jemalloc memory allocator V5.0.1 |
| Power Management: | -- |

### CPU

- **Name:** Intel Xeon Gold 6246
- **Max MHz:** 4200
- **Nominal:** 3300
- **Enabled:** 24 cores, 2 chips
- **Orderable:** 1.2 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **Cache L2:** 1 MB I+D on chip per core
- **Cache L3:** 24.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- **Storage:** 1 x 1.9 TB SSD SAS
- **Other:** None
## SPEC CPU®2017 Integer Speed Result

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### Results Table

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<td>605.mcf_s</td>
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<td>12.5</td>
<td>369</td>
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<td>377</td>
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<td>6.89</td>
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<td>110/12.9</td>
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<td>15.1</td>
<td>117/15.1</td>
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<td>270</td>
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<td>270</td>
<td>5.31</td>
<td>270/5.31</td>
<td>269/5.32</td>
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<td>5.14</td>
<td>332</td>
<td>5.14</td>
<td>332/5.14</td>
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<td>332</td>
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<td>17.9</td>
<td>163</td>
<td>18.0</td>
<td>163/18.0</td>
<td>24</td>
<td>163</td>
<td>18.0</td>
<td>164/18.0</td>
<td>164/17.9</td>
</tr>
</tbody>
</table>

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### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### General Notes

Environment variables set by runcpu before the start of the run:  
KMP_AFFINITY = "granularity=fine,scatter"  
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"  
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM  
memory using Redhat Enterprise Linux 7.5  
Transparent Huge Pages enabled by default  
Prior to runcpu invocation  
Filesystem page cache synced and cleared with:  
`sync; echo 3 > /proc/sys/vm/drop_caches`

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.  
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.  
jemalloc, a general purpose malloc implementation  
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5  
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SPEC CPU®2017 Integer Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

CPU2017 License: 9019
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SPECspeed®2017_int_base = 10.2
SPECspeed®2017_int_peak = 10.4

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-2vgg Sat Aug 31 13:34:37 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
  2 "physical id"s (chips)
  24 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 12
siblings : 12
  physical 0: cores 2 3 4 10 11 16 17 20 24 25 27
  physical 1: cores 0 2 4 8 9 10 11 17 18 19 25 27

From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 24
  On-line CPU(s) list: 0-23
  Thread(s) per core: 1
  Core(s) per socket: 12
  Socket(s): 2
  NUMA node(s): 2
  Vendor ID: GenuineIntel
  CPU family: 6
  Model: 85
  Model name: Intel(R) Xeon(R) Gold 6246 CPU @ 3.30GHz
  Stepping: 7
  CPU MHz: 3300.000
  CPU max MHz: 4200.0000
  CPU min MHz: 1200.0000
  BogoMIPS: 6600.00
  Virtualization: VT-x
  L1d cache: 32K
  L1i cache: 32K

(Continued on next page)
SPEC CPU®2017 Integer Speed Result

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Tested by: Cisco Systems

Platform Notes (Continued)

L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-11
NUMA node1 CPU(s): 12-23
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfmon perf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdmb fma cx16 xtrm pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt

/t proc/cpuinfo cache data
 cache size: 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
 available: 2 nodes (0-1)
 node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11
 node 0 size: 385635 MB
 node 0 free: 385131 MB
 node 1 cpus: 12 13 14 15 16 17 18 19 20 21 22 23
 node 1 size: 387028 MB
 node 1 free: 386534 MB
 node distances:
 node 0 1
 0: 10 21
 1: 21 10

From /proc/meminfo
 MemTotal: 791207884 kB
 HugePages_Total: 0
 Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
 os-release:
 NAME="SLES"
 VERSION="15"
 VERSION_ID="15"
 PRETTY_NAME="SUSE Linux Enterprise Server 15"
 ID="sles"
 ID_LIKE="suse"

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Platform Notes (Continued)

ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:

Linux linux-2vgg 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 31 13:32

SPEC is set to: /home/cpu2017

Filesystem  Type  Size  Used  Avail  Use% Mounted on
/dev/sdal   xfs  373G  16G  357G   5%  /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.3.34.0301190218 03/01/2019

Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C       | 600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
==============================================================================

C++      | 620.omnetpp_s(base, peak) 623.xalancbmk_s(base, peak) 631.deepsjeng_s(base, peak) 641.leela_s(base, peak)
==============================================================================
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6246, 3.30GHz)

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Compiler Version Notes (Continued)
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

---------------------------------------------------------------------
Fortran | 648.exchange2_s(base, peak)
---------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation
C benchmarks:
icc -m64 -std=c11
C++ benchmarks:
icpc -m64
Fortran benchmarks:
ifort -m64

Base Portability Flags
600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags
C benchmarks:
-W1, -z, muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

(Continued on next page)
**Cisco Systems**
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| SPECspeed®2017_int_base = 10.2 |
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### Base Optimization Flags (Continued)

C benchmarks (continued):
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

C++ benchmarks:
- `-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4`  
- `-I/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64 -lqkmalloc`

Fortran benchmarks:
- `-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4`  
- `-nostandard-realloc-lhs`

---

### Peak Compiler Invocation

C benchmarks:
- `icc -m64 -std=c11`

C++ benchmarks:
- `icpc -m64`

Fortran benchmarks:
- `ifort -m64`

---

### Peak Portability Flags

Same as Base Portability Flags

---

### Peak Optimization Flags

C benchmarks:
- `600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`  
- `-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3`  
- `-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp`  
- `-DSPEC_OPENMP -fno-strict-overflow`  
- `-L/usr/local/je5.0.1-64/lib -ljemalloc`

- `602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2`  
- `-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3`

(Continued on next page)
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Peak Optimization Flags (Continued)

602.gcc_s (continued):
-no-prec-div -DSPEC_SUPPRESS_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=4 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=4
-DSPEC_SUPPRESS_OPENMP
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

623.xalancbmk_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64
-lqkmalloc

631.deepsjeng_s: Same as 623.xalancbmk_s

641.leela_s: Same as 623.xalancbmk_s

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
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- Tested with SPEC CPU®2017 v1.0.5 on 2019-08-31 16:34:37-0400.
- Originally published on 2019-09-19.