**SPEC CPU®2017 Floating Point Rate Result**

Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

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<td>Cisco Systems</td>
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<tr>
<td>/spec CPU2017_fp_base =</td>
<td><strong>SPECrate®2017_fp_base =</strong></td>
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Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

**SPECS has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.**

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<td>564.chem3d_r</td>
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**Hardware**

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon Platinum 8253</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max MHz:</td>
<td>3000</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2200</td>
</tr>
<tr>
<td>Enabled:</td>
<td>32 cores, 2 chips, 2 threads/core</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
</tbody>
</table>

(Continued on next page)

**Software**

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Compiler:</td>
<td>C/C++; Version 19.0.4.227 of Intel C/C++ Compiler for Linux;</td>
</tr>
<tr>
<td></td>
<td>Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel:</td>
<td>No</td>
</tr>
</tbody>
</table>

(Continued on next page)

Page 1

Standard Performance Evaluation Corporation (info@spec.org)
https://www.spec.org/
SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Results Table

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

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**Operating System Notes**
Stack size set to unlimited using "ulimit -s unlimited"

**General Notes**
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

**Platform Notes**
BIOS Settings:
Intel HyperThreading Technology set to Enabled
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcded8f2999c33d61f64985e45859ea9
running on linux-3c6s Wed Aug 21 22:35:15 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

(Continued on next page)
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Platform Notes (Continued)

From /proc/cpuinfo

```
model name : Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
  2 "physical id"s (chips)
  64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
```

From lscpu:

```
Architecture:        x86_64
CPU op-mode(s):      32-bit, 64-bit
Byte Order:          Little Endian
CPU(s):              64
On-line CPU(s) list: 0-63
Thread(s) per core:  2
Core(s) per socket:  16
Socket(s):           2
NUMA node(s):        4
Vendor ID:           GenuineIntel
Family:              6
Model:               85
Model name:          Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
Stepping:            6
CPU MHz:             2200.000
CPU max MHz:         3000.000
CPU min MHz:         1000.000
BogoMIPS:            4400.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            22528K
NUMA node0 CPU(s):   0-3, 8-11, 32-35, 40-43
```

(Continued on next page)
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Platform Notes (Continued)

```
1:  11  10  21  21
2:  21  21  10  11
3:  21  21  11  10
```

From /proc/meminfo
MemTotal: 791198316 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release*/etc/*version*
```
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANCE_COLOR="0;32"
CFE_NAME="sle://suse:sles:15"
```

```
uname -a:
Linux linux-3c6s 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 21 12:58

SPEC is set to: /home/cpu2017
```
Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 224G 48G 176G 22% /
```

(Continued on next page)
Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Platinum 8253, 2.20GHz)

SPECrater2017_fp_base =

SPECrater2017_fp_peak =

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
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Platform Notes (Continued)

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
Memory:
24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
<table>
<thead>
<tr>
<th>C</th>
<th>519.lbm_r(base, peak) 538.imagick_r(base, peak) 544.nab_r(base, peak)</th>
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
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SPECrates

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Compiler Version Notes (Continued)

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C++, C, Fortran | 507.cactuBSSN_r(base, peak)
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran | 503.swaves_r(base, peak) 549.fotonik3d_r(base, peak)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
1985-2019 Intel Corporation. All rights reserved.

==============================================================================
Fortran C | 521.wrf_r(base, peak) 527.cam4_r(base, peak)
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## Base Compiler Invocation

**C benchmarks:**
```bash
icc -m64 -std=c11
```

**C++ benchmarks:**
```bash
icpc -m64
```

**Fortran benchmarks:**
```bash
ifort -m64
```

**Benchmarks using both Fortran and C:**
```bash
ifort -m64 icc -m64 -std=c11
```

**Benchmarks using both C and C++:**
```bash
icpc -m64 icc -m64 -std=c11
```

**Benchmarks using Fortran, C, and C++:**
```bash
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64

Non-Compliant
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---

**Base Optimization Flags**

C benchmarks:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
- -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -auto
- -nostandard-realloc-lhs -align array32byte

---

**Peak Compiler Invocation**

C benchmarks:
- icc -m64 -std=c11

C++ benchmarks:
- icpc -m64

(Continued on next page)
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Peak Compiler Invocation (Continued)

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
519.ibm_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

538.imagick_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

544.nab_r: Same as 538.imagick_r

(Continued on next page)
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**Peak Optimization Flags (Continued)**

C++ benchmarks:

508.namd_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

510.parest_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

**Fortran benchmarks:**

503.bwaves_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

549.fotonik3d_r: Same as 503.bwaves_r

554.roms_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:

511.povray_r: -prof-gen(pass 1) -prof-use(pass 2) -ipo -xCORE-AVX512 -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

526.blender_r: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4

(Continued on next page)
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Peak Optimization Flags (Continued)

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -ipo -reftoch
-ffinite-math-only -qopt-mem-layout-trans=3 -auto
-nostandard-realloc-lhs -align-array-2byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links: