Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6252, 2.10GHz)

SPECrater®2017_fp_base = 237
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

<table>
<thead>
<tr>
<th>Software</th>
<th>Hardware</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name: Intel Xeon Gold 6252</td>
<td>OS: SUSE Linux Enterprise Server 15 (x86_64)</td>
</tr>
<tr>
<td>Max MHz: 3700</td>
<td>4.12.14-23-default</td>
</tr>
<tr>
<td>Nominal: 2100</td>
<td>Compiler: C/C++: Version 19.0.4.227 of Intel C/C++</td>
</tr>
<tr>
<td>Enabled: 48 cores, 2 chips, 2 threads/core</td>
<td>Compiler for Linux;</td>
</tr>
<tr>
<td>Orderable: 1,2 Chips</td>
<td>Fortran: Version 19.0.4.227 of Intel Fortran</td>
</tr>
<tr>
<td>Cache L1: 32 KB I + 32 KB D on chip per core</td>
<td>Compiler for Linux</td>
</tr>
<tr>
<td>L2: 1 MB I+D on chip per core</td>
<td>Parallel: No</td>
</tr>
<tr>
<td>L3: 35.75 MB I+D on chip per chip</td>
<td>Firmware: Version 4.0.4b released Apr-2019</td>
</tr>
<tr>
<td>Other: None</td>
<td>File System: btrfs</td>
</tr>
<tr>
<td>Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
<td>System State: Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Storage: 1 x 240 GB M.2 SATA SSD</td>
<td>Base Pointers: 64-bit</td>
</tr>
<tr>
<td>Other: None</td>
<td>Peak Pointers: Not Applicable</td>
</tr>
<tr>
<td>Power Management: --</td>
<td>Other: None</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6252, 2.10GHz)

SPECrate®2017_fp_base = 237
SPECrate®2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>96</td>
<td>1817</td>
<td>530</td>
<td>1819</td>
<td>529</td>
<td>1818</td>
<td>529</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>96</td>
<td>606</td>
<td>201</td>
<td>604</td>
<td>201</td>
<td>604</td>
<td>201</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>96</td>
<td>471</td>
<td>194</td>
<td>470</td>
<td>194</td>
<td>470</td>
<td>194</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>96</td>
<td>1936</td>
<td>130</td>
<td>1947</td>
<td>129</td>
<td>1932</td>
<td>130</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>96</td>
<td>784</td>
<td>286</td>
<td>783</td>
<td>286</td>
<td>782</td>
<td>286</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>96</td>
<td>794</td>
<td>127</td>
<td>794</td>
<td>127</td>
<td>793</td>
<td>128</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>96</td>
<td>904</td>
<td>238</td>
<td>929</td>
<td>232</td>
<td>905</td>
<td>238</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>96</td>
<td>560</td>
<td>261</td>
<td>560</td>
<td>261</td>
<td>560</td>
<td>261</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>96</td>
<td>580</td>
<td>290</td>
<td>588</td>
<td>286</td>
<td>573</td>
<td>293</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>96</td>
<td>409</td>
<td>583</td>
<td>407</td>
<td>586</td>
<td>409</td>
<td>584</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>96</td>
<td>381</td>
<td>424</td>
<td>379</td>
<td>426</td>
<td>377</td>
<td>429</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>96</td>
<td>2203</td>
<td>170</td>
<td>2203</td>
<td>170</td>
<td>2202</td>
<td>170</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>96</td>
<td>1511</td>
<td>101</td>
<td>1511</td>
<td>101</td>
<td>1511</td>
<td>101</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) (Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6252, 2.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECrate®2017_fp_base = 237
SPECrate®2017_fp_peak = Not Run

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

General Notes (Continued)

is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Enabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Enabled
IMC Interleaving set to 1-way Interleave
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b091c0f
running on linux-pmqx Fri Aug 23 20:23:03 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6252 CPU @ 2.10GHz
  2 "physical id"s (chips)
  96 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 48
physical 0: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 8 9 10 12 13 16 17 18 19 20 21 22 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 96
On-line CPU(s) list: 0-95
Thread(s) per core: 2
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Cisco Systems  
Cisco UCS B200 M5 (Intel Xeon Gold 6252, 2.10GHz)

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

SPECrate®2017_fp_base = 237
SPECrate®2017_fp_peak = Not Run

Test Date: Aug-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

Platform Notes (Continued)

Model: 85  
Model name: Intel(R) Xeon(R) Gold 6252 CPU @ 2.10GHz  
Stepping: 6  
CPU MHz: 2100.000  
CPU max MHz: 3700.0000  
CPU min MHz: 1000.0000  
BogoMIPS: 4200.00  
Virtualization: VT-x  
L1d cache: 32K  
L1i cache: 32K  
L2 cache: 1024K  
L3 cache: 36608K  
NUMA node0 CPU(s): 0-3,7,8,12-14,18-20,48-51,55,56,60-62,66-68  
NUMA node1 CPU(s): 4-6,9-11,15-17,21-23,52-54,57-59,63-65,69-71  
NUMA node2 CPU(s): 24-27,31-33,36-38,43,44,72-75,79-81,84-86,91,92  
NUMA node3 CPU(s): 28-30,34,35,39-42,45-47,76-78,82,83,87-90,93-95  
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdemsg rdtsscp lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperf perfctr tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single intel_pinn tpr_shadow vnmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2  invpcid rtm cqm mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsave xstate xgetbv1 xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local ibpb ibrs stibp dtherm ida arat pln pts hwp hwp_act_window hwp_epp hwp_pkg_req pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data  
cache size : 36608 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.  
available: 4 nodes (0-3)  
node 0 cpus: 0 1 2 3 7 8 12 13 14 18 19 20 48 49 50 51 55 56 60 61 62 66 67 68  
node 0 size: 192090 MB  
node 0 free: 185216 MB  
node 1 cpus: 4 5 6 9 10 11 15 16 17 21 22 23 52 53 54 57 58 59 63 64 65 69 70 71  
node 1 size: 193521 MB  
node 1 free: 188014 MB  
node 2 cpus: 24 25 26 27 31 32 33 36 37 38 43 44 72 73 74 75 79 80 81 84 85 86 91 92  
node 2 size: 193492 MB  
node 2 free: 188388 MB  
node 3 cpus: 28 29 30 34 35 39 40 41 42 45 46 47 76 77 78 82 83 87 88 89 90 93 94 95  
node 3 size: 193518 MB  
node 3 free: 188401 MB

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6252, 2.10GHz)

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Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

node distances:
node  0 1 2 3
0: 10 11 21 21
1: 11 10 21 21
2: 21 21 10 11
3: 21 21 11 10

From /proc/meminfo
MemTotal: 791164564 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
  Linux linux-pmqx 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 23 15:40

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 btrfs 169G 35G 134G 21% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
  Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6252, 2.10GHz)

SPECrater®2017_fp_base = 237
SPECrater®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes

==============================================================================
C               | 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++             | 508.namd_r(base) 510.parest_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C          | 511.povray_r(base) 526.blender_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 507.cactuBSSN_r(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran         | 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6252, 2.10GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_fp_base</th>
<th>237</th>
</tr>
</thead>
<tbody>
<tr>
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<td>Not Run</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor</td>
<td>Cisco Systems</td>
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<tr>
<td>Tested by</td>
<td>Cisco Systems</td>
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<tr>
<td>Test Date</td>
<td>Aug-2019</td>
</tr>
<tr>
<td>Hardware Availability</td>
<td>Apr-2019</td>
</tr>
<tr>
<td>Software Availability</td>
<td>May-2019</td>
</tr>
</tbody>
</table>

Compiler Version Notes (Continued)

```plaintext
Fortran, C      | 521.wrf_r(base) 527.cam4_r(base)
---              |-----------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

Base Compiler Invocation

C benchmarks:
```plaintext
icc -m64 -std=c11
```
C++ benchmarks:
```plaintext
icpc -m64
```
Fortran benchmarks:
```plaintext
ifort -m64
```
Benchmarks using both Fortran and C:
```plaintext
ifort -m64 icc -m64 -std=c11
```
Benchmarks using both C and C++:
```plaintext
icpc -m64 icc -m64 -std=c11
```
Benchmarks using Fortran, C, and C++:
```plaintext
icpc -m64 icc -m64 -std=c11 ifort -m64
```

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
```
(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6252, 2.10GHz)

SPECratenumber2017_fp_base = 237
SPECratenumber2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
CPU2017 License: 9019
Tested by: Cisco Systems
Hardware Availability: Apr-2019

Base Portability Flags (Continued)

527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
538.imagick_r: -DSPEC_LP64
544.nab_r: -DSPEC_LP64
549.fotonik3d_r: -DSPEC_LP64
554.roms_r: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

Benchmarks using both C and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -auto
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6252, 2.10GHz)

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