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<table>
<thead>
<tr>
<th>Threads</th>
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<tbody>
<tr>
<td>603.bwaves_s</td>
<td></td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td></td>
</tr>
<tr>
<td>619.lbm_s</td>
<td></td>
</tr>
<tr>
<td>621.wrf_s</td>
<td></td>
</tr>
<tr>
<td>627.cam4_s</td>
<td></td>
</tr>
<tr>
<td>628.pop2_s</td>
<td></td>
</tr>
<tr>
<td>638.imagick_s</td>
<td></td>
</tr>
<tr>
<td>644.nab_s</td>
<td></td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td></td>
</tr>
<tr>
<td>654.roms_s</td>
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<table>
<thead>
<tr>
<th>Hardware</th>
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<tbody>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Platinum 8253</td>
</tr>
<tr>
<td>Max MHz:</td>
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</tr>
<tr>
<td>Nominal:</td>
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<tr>
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<tr>
<td>Cache L1:</td>
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<tr>
<td>L2:</td>
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<td>L3:</td>
<td>22 MB I+D on chip per chip</td>
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<table>
<thead>
<tr>
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<tr>
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<td>SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
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<td>Peak Pointers:</td>
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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

SPECSpeed®2017_fp_base =
SPECSpeed®2017_fp_peak =

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

Results Table

<table>
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<th>Seconds</th>
<th>Ratio</th>
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<td>NC</td>
<td>NC</td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base =
SPECspeed®2017_fp_peak =

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

| SPECspeed®2017_fp_base = |
| SPECspeed®2017_fp_peak = |

CPU2017 License: 9019  
Test Sponsor: Cisco Systems  
Tested by: Cisco Systems

Test Date: Jul-2019  
Hardware Availability: Apr-2019  
Software Availability: May-2019

SPEC has determined that this result does not comply with the SPEC OSG Guidelines for General Availability and the SPEC CPU 2017 run and reporting rules. Specifically, the submitter has notified SPEC that the system was run with a CPU that is not supported by Cisco with the given system configuration.

General Notes (Continued)
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Sysinfo program /home/cpu2017/bin/sysinfo

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
- model name : Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
- physical id"s (chips)
  32 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 16
  siblings : 16
  physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
  physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 32

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

### SPEC CPU 2017 Floating Point Speed Result

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_peak</th>
<th>SPECspeed®2017_fp_base</th>
</tr>
</thead>
</table>

Specified Copyright 2017-2020

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jul-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Jul-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

**Platform Notes (Continued)**

- On-line CPU(s) list: 0-31
- Thread(s) per core: 1
- Core(s) per socket: 16
- Vendor ID: GenuineIntel
- Model: 85
- Model name: Intel(R) Xeon(R) Platinum 8253 CPU @ 2.20GHz
- Stepping: 6
- CPU MHz: 2200.000
- CPU max MHz: 3000.0000
- CPU min MHz: 1000.0000
- BogoMIPS: 4400.00
- Virtualization: VT-x
- L1d cache: 32K
- L1i cache: 32K
- L2 cache: 1024K
- L3 cache: 22528K
- NUMA node0 CPU(s): 0-15
- NUMA node1 CPU(s): 16-31
- Flags: fpu vme de pse mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc tsc_adjust mipsart arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault est cat_l3 cdp cdf l1d tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault est cat_l3 cdp l1d

Non-Compliant

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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

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Platform Notes (Continued)

From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.
available: 2 nodes (0-1)
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
node 0 size: 385429 MB
node 0 free: 381852 MB
node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
node 1 size: 387045 MB
node 1 free: 381015 MB
node distances:
node   0   1
0:  10  21
1:  21  10

From /proc/meminfo
MemTotal: 791014168 kB
HugePages_Total: 0
Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
Linux linux-db10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
Platform Notes

Non-Compliant

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Guidelines for General Availability

Non-Compliant

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Platform Notes (Continued)

Additional information from the sysinfo program follows. WARNING: Use caution when you interpret this section. The 'sdc' command reads system data which is intended to allow hardware to be accurately determined, but the intent may not be met, as there are frequent changes to the hardware and the 'DMT' SMBIOS standard.

---

Compiler Version Notes

---

Non-Compliant

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Compiler Version Notes (Continued)

Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

(Continued on next page)
SPECSPEC CPU®2017 Floating Point Speed Result

Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8253, 2.20GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_peak</th>
<th>SPECspeed®2017_fp_base</th>
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

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Base Compiler Invocation (Continued)

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 tcl -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
   -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -03 -no-prec-div -qopt-prefetch

(Continued on next page)
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Base Optimization Flags (Continued)

Benchmarks using both Fortran and C (continued):
-ffinite-math-only -qopt-mem-layout=trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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