Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base = 154</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak = Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base (154)</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s 56</td>
<td>0 20.0 50.0 80.0 100 120 140 160 180 200 220 240 260 280 300 320 340 360 380 400 420 440 460 480 500 520 540 560</td>
</tr>
<tr>
<td>607.cactuBSSN_s 56</td>
<td>105</td>
</tr>
<tr>
<td>619.lbm_s 56</td>
<td>130</td>
</tr>
<tr>
<td>621.wrf_s 56</td>
<td>126</td>
</tr>
<tr>
<td>627.cam4_s 56</td>
<td>62.3</td>
</tr>
<tr>
<td>628.pop2_s 56</td>
<td>167</td>
</tr>
<tr>
<td>638.imagick_s 56</td>
<td>84.5</td>
</tr>
<tr>
<td>644.nab_s 56</td>
<td>321</td>
</tr>
<tr>
<td>649.fotonik3d_s 56</td>
<td>166</td>
</tr>
<tr>
<td>654.roms_s 56</td>
<td>--</td>
</tr>
</tbody>
</table>

**Hardware**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name:</td>
<td>Intel Xeon Platinum 8280M</td>
</tr>
<tr>
<td>Max MHz:</td>
<td>4000</td>
</tr>
<tr>
<td>Nominal:</td>
<td>2700</td>
</tr>
<tr>
<td>Enabled:</td>
<td>56 cores, 2 chips</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I+ 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>38.5 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 240 GB M.2 SATA SSD</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
</tbody>
</table>

**Software**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>OS:</td>
<td>SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default</td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel:</td>
<td>Yes</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 4.0.4b released Apr-2019</td>
</tr>
<tr>
<td>File System:</td>
<td>btrfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>Not Applicable</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Power Management:</td>
<td>--</td>
</tr>
</tbody>
</table>
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>56</td>
<td>119</td>
<td>496</td>
<td>119</td>
<td>497</td>
<td>119</td>
<td>496</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>56</td>
<td>90.4</td>
<td>184</td>
<td>90.8</td>
<td>184</td>
<td>91.1</td>
<td>183</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>56</td>
<td>49.7</td>
<td>105</td>
<td>49.9</td>
<td>105</td>
<td>49.9</td>
<td>105</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>56</td>
<td>102</td>
<td>130</td>
<td>101</td>
<td>130</td>
<td>101</td>
<td>131</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>56</td>
<td>70.4</td>
<td>126</td>
<td>70.9</td>
<td>125</td>
<td>70.5</td>
<td>126</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>56</td>
<td>191</td>
<td>62.1</td>
<td>191</td>
<td>62.3</td>
<td>191</td>
<td>62.3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>56</td>
<td>86.1</td>
<td>168</td>
<td>86.3</td>
<td>167</td>
<td>86.2</td>
<td>167</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>644.nab_s</td>
<td>56</td>
<td>54.4</td>
<td>321</td>
<td>54.3</td>
<td>322</td>
<td>54.4</td>
<td>321</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>56</td>
<td>108</td>
<td>84.5</td>
<td>108</td>
<td>84.8</td>
<td>108</td>
<td>84.4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>654.roms_s</td>
<td>56</td>
<td>94.8</td>
<td>166</td>
<td>95.0</td>
<td>166</td>
<td>94.9</td>
<td>166</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 154
SPECspeed®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/lib/ia32:/home/cpu2017/je5.0.1-32"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3>/proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes
BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>154</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

---

## Platform Notes (Continued)

Power Performance Tuning set to OS Controls  
SNC set to Disabled  
IMC Interleaving set to Auto  
Sysinfo program /home/cpu2017/bin/sysinfo  
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bccc091c0f  
running on linux-pmqx Sat Aug 31 17:32:43 2019

SUT (System Under Test) info as seen by some common utilities.  
For more information on this section, see  
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

```plaintext
model name : Intel(R) Xeon(R) Platinum 8280M CPU @ 2.70GHz
  2  "physical id"s (chips)
  56 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 28
siblings : 28
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
physical 1: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 14 16 17 18 19 20 21 22 24 25 26 27 28 29 30
```

From lscpu:

```plaintext
Architecture:  x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 56
On-line CPU(s) list: 0-55
Thread(s) per core: 1
Core(s) per socket: 28
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8280M CPU @ 2.70GHz
Stepping: 6
CPU MHz: 2700.000
CPU max MHz: 4000.0000
CPU min MHz: 1000.0000
BogoMIPS: 5400.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
```

(Continued on next page)
Cisco Systems

Cisco UCS B200 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>154</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

| L3 cache:    | 39424K |
| NUMA node0 CPU(s): | 0-27 |
| NUMA node1 CPU(s): | 28-55 |

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.

From /proc/cpuinfo cache data

```plaintext
Cache size : 39424 KB
```

From /proc/meminfo

```plaintext
MemTotal:       791172588 kB
HugePages_Total:       0
Hugepagesize:       2048 kB
```

From /etc/*release* /etc/*version*

```plaintext
os-release:
NAME="SLES"
VERSION="15"
VERSION_ID="15"
PRETTY_NAME="SUSE Linux Enterprise Server 15"
ID="sles"
ID_LIKE="suse"
```

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

SPECspeed®2017_fp_base = 154
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux linux-pmqx 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 31 12:00

SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4      btrfs  169G   22G  147G  13% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
    Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8280M, 2.70GHz)

SPECspeed®2017_fp_base = 154
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Compiler Version Notes (Continued)

==============================================================================
Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
Fortran, C      | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl

(Continued on next page)
## Cisco Systems

**Cisco UCS B200 M5** (Intel Xeon Platinum 8280M, 2.70GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>154</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Base Portability Flags (Continued)

- 638.imagick_s: -DSPEC_LP64
- 644.nab_s: -DSPEC_LP64
- 649.fotonik3d_s: -DSPEC_LP64
- 654.roms_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

**Fortran benchmarks:**

-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
-nostandard-realloc-lhs

**Benchmarks using both Fortran and C:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs

**Benchmarks using Fortran, C, and C++:**

-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-08-31 20:32:43-0400.


Originally published on 2019-09-19.