Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6254, 3.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Threads

603.bwaves_s 36
607.cactuBSSN_s 36
619.lbm_s 36
621.wrf_s 36
627.cam4_s 36
628.pop2_s 36
638.imagick_s 36
644.nab_s 36
649.fotonik3d_s 36
654.roms_s 36

Hardware
CPU Name: Intel Xeon Gold 6254
Max MHz: 4000
Nominal: 3100
Enabled: 36 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 240 GB M.2 SATA SSD
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
4.12.14-23-default
Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4b released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
Power Management: --
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6254, 3.10GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Base</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Peak</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>36</td>
<td>111</td>
<td>533</td>
<td>110</td>
<td>536</td>
<td>111</td>
<td>534</td>
<td></td>
<td></td>
</tr>
<tr>
<td>607.cactuBSSN_s</td>
<td>36</td>
<td>104</td>
<td>160</td>
<td>104</td>
<td>160</td>
<td>105</td>
<td>159</td>
<td></td>
<td></td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>36</td>
<td>51.3</td>
<td>102</td>
<td>50.9</td>
<td>103</td>
<td>51.0</td>
<td>103</td>
<td></td>
<td></td>
</tr>
<tr>
<td>621.wrf_s</td>
<td>36</td>
<td>96.1</td>
<td>138</td>
<td>96.3</td>
<td>137</td>
<td>95.7</td>
<td>138</td>
<td></td>
<td></td>
</tr>
<tr>
<td>627.cam4_s</td>
<td>36</td>
<td>86.7</td>
<td>102</td>
<td>87.0</td>
<td>102</td>
<td>86.5</td>
<td>102</td>
<td></td>
<td></td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>36</td>
<td>174</td>
<td>68.2</td>
<td>175</td>
<td>68.0</td>
<td>171</td>
<td>69.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>36</td>
<td>119</td>
<td>121</td>
<td>120</td>
<td>120</td>
<td>116</td>
<td>125</td>
<td></td>
<td></td>
</tr>
<tr>
<td>644.nab_s</td>
<td>36</td>
<td>66.3</td>
<td>264</td>
<td>66.2</td>
<td>264</td>
<td>66.2</td>
<td>264</td>
<td></td>
<td></td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>36</td>
<td>107</td>
<td>84.9</td>
<td>108</td>
<td>84.7</td>
<td>108</td>
<td>84.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>654.roms_s</td>
<td>36</td>
<td>127</td>
<td>124</td>
<td>128</td>
<td>123</td>
<td>129</td>
<td>122</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SPECspeed®2017_fp_base = 140
SPECspeed®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6254, 3.10GHz)

SPECspeed®2017_fp_base = 140
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-bo6o Wed Aug 28 21:01:11 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo:
  model name : Intel(R) Xeon(R) Gold 6254 CPU @ 3.10GHz
  2 "physical id"s (chips)
  36 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following
  excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
  cpu cores : 18
  siblings : 18
  physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
  physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
  Architecture: x86_64
  CPU op-mode(s): 32-bit, 64-bit
  Byte Order: Little Endian
  CPU(s): 36
  On-line CPU(s) list: 0-35
  Thread(s) per core: 1
  Core(s) per socket: 18
  Socket(s): 2
  NUMA node(s): 2
  Vendor ID: GenuineIntel
  CPU family: 6
  Model: 85
  Model name: Intel(R) Xeon(R) Gold 6254 CPU @ 3.10GHz
  Stepping: 6
  CPU MHz: 3100.000
  CPU max MHz: 4000.0000
  CPU min MHz: 1200.0000
  BogoMIPS: 6200.00
  Virtualization: VT-x
  L1d cache: 32K
  L1i cache: 32K
  L2 cache: 1024K
  L3 cache: 25344K

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6254, 3.10GHz)

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base</th>
<th>140</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Platform Notes (Continued)

NUMA node0 CPU(s):   0-17
NUMA node1 CPU(s):   18-35
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl noapo mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl noapo mca cmov
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl noapo mca cmov

/proc/cpuinfo cache data
    cache size : 25344 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
    physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
    node 0 size: 385428 MB
    node 0 free: 384430 MB
    node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35
    node 1 size: 387045 MB
    node 1 free: 378424 MB

From /proc/meminfo
    MemTotal:      791013368 kB
    HugePages_Total:       0
    Hugepagesize:        2048 kB

From /etc/*release* /etc/*version*
    os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6254, 3.10GHz)

SPECspeed®2017_fp_base = 140
SPECspeed®2017_fp_peak = Not Run

Platform Notes (Continued)

uname -a:
    Linux linux-bo6o 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 28 15:31

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sdb1 btrfs 224G 22G 202G 10% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
    Memory:
        24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

==============================================================================
C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

(Continued on next page)
Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6254, 3.10GHz)

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Aug-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: May-2019</td>
</tr>
</tbody>
</table>

**Compiler Version Notes (Continued)**

<table>
<thead>
<tr>
<th>Fortran</th>
<th>603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Fortran, C</th>
<th>621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 Copyright (C) 1985-2019 Intel Corporation. All rights reserved. Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416 Copyright (C) 1985-2019 Intel Corporation. All rights reserved.</td>
<td></td>
</tr>
</tbody>
</table>

**Base Compiler Invocation**

C benchmarks:
```bash
c -m64 -std=c11
```

Fortran benchmarks:
```bash
ifort -m64
```

Benchmarks using both Fortran and C:
```bash
ifort -m64 icc -m64 -std=c11
```

Benchmarks using Fortran, C, and C++:
```bash
icpc -m64 icc -m64 -std=c11 ifort -m64
```

**Base Portability Flags**

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64

(Continued on next page)
# SPEC CPU®2017 Floating Point Speed Result

## Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Gold 6254, 3.10GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SPECspeed®2017_fp_base =</th>
<th>140</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_fp_peak =</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
**Software Availability:** May-2019

### Base Portability Flags (Continued)

- 649.fotonik3d_s: -DSPEC_LP64
- 654.roms_s: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

**Fortran benchmarks:**
- -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
- -nostandard-realloc-lhs

**Benchmarks using both Fortran and C:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
- -nostandard-realloc-lhs

**Benchmarks using Fortran, C, and C++:**
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
- -ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
- -nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at:

You can also download the XML flags sources by saving the following links:

---

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-08-29 00:01:10-0400.  
Originally published on 2019-09-19.

Page 7

Standard Performance Evaluation Corporation (info@spec.org)  
https://www.spec.org/