Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)

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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

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</table>

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SPECspeed®2017_int_base (10.4)

Hardware

### CPU
- Name: Intel Xeon Platinum 8260
- Max MHz: 3900
- Nominal: 2400
- Enabled: 48 cores, 2 chips
- Orderable: 1, 2 chip(s)
- Cache L1: 32 KB I + 32 KB D on chip per core
- L2: 1 MB I+D on chip per core
- L3: 35.75 MB I+D on chip per chip
- Other: None
- Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
- Storage: 1 x 960 GB SATA M.2 SSD
- Other: None

### Memory
- None

Software

- OS: SUSE Linux Enterprise Server 15 (x86_64) 4.12.14-23-default
- Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
- Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
- Parallel: Yes
- Firmware: Version 4.0.4b released Apr-2019
- File System: xfs
- System State: Run level 3 (multi-user)
- Base Pointers: 64-bit
- Peak Pointers: Not Applicable
- Other: jemalloc memory allocator V5.0.1
- Power Management: --

Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019
Results Table

<table>
<thead>
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</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,scatter"
LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64:/home/cpu2017/je5.0.1-64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
    sync; echo 3> /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
SPEC CPU®2017 Integer Speed Result
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Cisco Systems
Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)

SPECspeed®2017_int_base = 10.4
SPECspeed®2017_int_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
Tested by: Cisco Systems
Hardware Availability: Apr-2019
Software Availability: May-2019

Platform Notes

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
IMC Interleaving set to Auto
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
running on linux-3xnd Fri Aug 23 09:02:29 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Platinum 8260 CPU @ 2.40GHz
  2 "physical id"s (chips)
  48 "processors"
core , siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 6 8 9 10 11 12 13 16 17 18 19 20 21 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 6 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Platinum 8260 CPU @ 2.40GHz
Stepping: 6
CPU MHz: 2400.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 4800.00
Virtualization: VT-x
L1d cache: 32K

(Continued on next page)
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**SPEC CPU®2017 Integer Speed Result**

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### Cisco Systems

**Cisco UCS B200 M5 (Intel Xeon Platinum 8260, 2.40GHz)**

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**CPU2017 License:** 9019  
**Test Date:** Aug-2019  
**Test Sponsor:** Cisco Systems  
**Hardware Availability:** Apr-2019  
**Tested by:** Cisco Systems  
**Software Availability:** May-2019

---

**Platform Notes (Continued)**

- **L1i cache:** 32K
- **L2 cache:** 1024K
- **L3 cache:** 36608K
- **NUMA node0 CPU(s):** 0-23
- **NUMA node1 CPU(s):** 24-47
- **Flags:**  
  - fpu  
  - vme  
  - de  
  - pse  
  - msr  
  - mca  
  - cmov  
  - pat  
  - pse36  
  - clflush  
  - dts  
  - acpi  
  - mmx  
  - fxsr  
  - sse  
  - sse2  
  - ss  
  - ht  
  - tsc  
  - mce  
  - cx8  
  - apic  
  - sep  
  - mtrr  
  - pae  
  - cmov  
  - cx16  
  - x86tr  
  - pdcm  
  - pcd  
  - sse4_1  
  - sse4_2  
  - x2apic  
  - movbe  
  - popcnt  
  - tsc_deadline_timer  
  - aes  
  - xsave  
  - avx  
  - f16c  
  - rdrand  
  - lahf_lm  
  - abm  
  - 3dnowprefetch  
  - cpuid_fault  
  - epb  
  - cat_l3  
  - invd  
  - single  
  - intel_puin  
  - tpr_shadow  
  - vnumi  
  - flexpriority  
  - ept  
  - vpid  
  - fsqsb  
  - base  
  - tsc_adjust  
  - bm  
  - hl  
  - e  
  -  
  - avx2  
  - smep  
  - bmi2  
  - erms  
  - invpcid  
  - rt  
  - cmq  
  - mpx  
  - rdrt  
  - a  
  - avx512f  
  - avx512dq  
  - rseed  
  - ax  
  - smp  
  - clflushopt  
  - clwb  
  - intel_pt  
  - avx512cd  
  - avx512bw  
  - avx512vl  
  - xsaveopt  
  - xsavec  
  - xsave  
  - cqm  
  - l1c  
  - cqm  
  - occcup  
  - llc  
  - cqm_mbm_total  
  - cqm_mbm_local  
  - ibp  
  - b  
  - ibrs  
  - dtb  
  - h  
  - ida  
  - ar  
  - at  
  - pln  
  - pts  
  - hwp  
  - hwp_act_window  
  - hwp_epp  
  - hwp_pkg_req  
  - pkt  
  - ospe  
  - avx512_vnni  
  - arch_capabilities  
  - ssbd  

---

From `numactl --hardware` WARNING: a numactl 'node' might or might not correspond to a physical chip.

### Available:

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From `/proc/meminfo`

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</tr>
<tr>
<td>Hugepagesize</td>
<td>4096 kB</td>
</tr>
</tbody>
</table>

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From `/etc/*release*`/`/etc/*version*`

### os-release:

- NAME="SLES"  
- VERSION="15"  
- VERSION_ID="15"  
- PRETTY_NAME="SUSE Linux Enterprise Server 15"  
- ID="sles"

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(Continued on next page)
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CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Aug-2019
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Test Sponsor: Cisco Systems
Test Date: Aug-2019

Platform Notes (Continued)

uname -a:
  Linux linux-3xnd 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Aug 23 06:40
SPEC is set to: /home/cpu2017
Filesystem Type Size Used Avail Use% Mounted on
/dev/sdb4 xfs 100G 16G 85G 16% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
  BIOS Cisco Systems, Inc. B200M5.4.0.4b.0.0407191258 04/07/2019
  Memory:
  24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

C
600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base)
625.x264_s(base) 657.xz_s(base)

C++
620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)
641.leela_s(base)

Fortran
648.exchange2_s(base)

(Continued on next page)
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Compiler Version Notes (Continued)

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-W1,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=4
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.4.227/linux/compiler/lib/intel64

(Continued on next page)
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#### Base Optimization Flags (Continued)

**C++ benchmarks (continued):**  
- -lqkmalloc

**Fortran benchmarks:**  
- -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
- -nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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Originally published on 2019-09-19.