Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Aug-2019
Hardware Availability: Apr-2019
Software Availability: May-2019

Threads

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<th>SPECspeed®2017_fp_peak (132)</th>
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<tr>
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<tr>
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<tr>
<td>628.pop2_s</td>
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<tr>
<td>638.imagick_s</td>
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<tr>
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<tr>
<td>654.roms_s</td>
<td>36</td>
<td>90.3</td>
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</tbody>
</table>

Hardware

CPU Name: Intel Xeon Gold 6240M
Max MHz: 3900
Nominal: 2600
Enabled: 36 cores, 2 chips
Orderable: 1.2 Chips
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 24.75 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933V-R)
Storage: 1 x 1.9 TB SSD SAS
Other: None

Software

Compiler: C/C++: Version 19.0.4.227 of Intel C/C++ Compiler for Linux;
                      Fortran: Version 19.0.4.227 of Intel Fortran Compiler for Linux
Parallel: Yes
Firmware: Version 4.0.4d released May-2019
File System: xfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: 64-bit
Other: None
Power Management: --
## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)  

### SPEC CPU 2017 Floating Point Speed Result

**SPECspeed®2017_fp_base** = 132  
**SPECspeed®2017_fp_peak** = 132

---

### Results Table

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<td><strong>130</strong></td>
</tr>
</tbody>
</table>

**SPECspeed®2017_fp_base** = 132  
**SPECspeed®2017_fp_peak** = 132

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

---

### General Notes

Environment variables set by runcpu before the start of the run:

- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation:

- Filesystem page cache synced and cleared with:
  - sync; echo 3 > /proc/sys/vm/drop_caches

NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

---

### Platform Notes

- BIOS Settings:
  - Intel HyperThreading Technology set to Disabled
  - CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)  SPECspeed®2017_fp_base = 132  SPECspeed®2017_fp_peak = 132

CPU2017 License: 9019  Test Date: Aug-2019
Test Sponsor: Cisco Systems  Hardware Availability: Apr-2019
Tested by: Cisco Systems  Software Availability: May-2019

Platform Notes (Continued)

Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bce8f2999c33d61f64985e45859ea9
running on linux-3c6s Wed Aug 7 23:29:10 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz
  2 "physical id"s (chips)
  36 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 18
siblings : 18
physical 0: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27
physical 1: cores 0 1 2 3 4 8 9 10 11 16 17 18 19 20 24 25 26 27

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 36
On-line CPU(s) list: 0-35
Thread(s) per core: 1
Core(s) per socket: 18
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 6240M CPU @ 2.60GHz
Stepping: 7
CPU MHz: 2600.000
CPU max MHz: 3900.0000
CPU min MHz: 1000.0000
BogoMIPS: 5200.00
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 25344K
NUMA node0 CPU(s): 0-17

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)

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**Test Date:** Aug-2019  
**Hardware Availability:** Apr-2019  
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**Platform Notes (Continued)**

```
NUMA node1 CPU(s): 18-35
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperfperf tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdbg fma cx16 xtrnr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
```

```
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cpd_13 invpcid_single intel_puin mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ills invpcid rdt_a
```

```
From numactl --hardware  WARNING: a numactl 'node' might or might not correspond to a physical chip.  
available: 2 nodes (0-1)  
node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17  
ode 0 size: 385604 MB  
ode 0 free: 385189 MB  
node 1 cpus: 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35  
ode 1 size: 387056 MB  
ode 1 free: 379411 MB  
node distances:  
ode 0 1  
0: 10 21  
1: 21 10
```

```
From /proc/meminfo  
MemTotal: 791204640 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB
```

```
From /etc/*release* /etc/*version*  
```
```
NAME="SLES"  
VERSION="15"  
VERSION_ID="15"  
PRETTY_NAME="SUSE Linux Enterprise Server 15"  
ID="sles"  
ID_LIKE="suse"  
ANSI_COLOR="0;32"  
CPE_NAME="cpe:/o:suse:sles:15"
```

(Continued on next page)
Cisco Systems
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| SPECspeed®2017_fp_base = 132 |
| SPECspeed®2017_fp_peak = 132 |

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<td>May-2019</td>
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</table>

Platform Notes (Continued)

uname -a:
    Linux linux-3c6s 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Aug 7 18:57

SPEC is set to: /home/cpu2017
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sda1 xfs 224G 26G 198G 12% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

    BIOS Cisco Systems, Inc. C240M5.4.0.4d.0.0506190827 05/06/2019
    Memory:
    24x 0xCE00 M393A4K40CB2-CVF 32 GB 2 rank 2933, configured at 2934

(End of data from sysinfo program)

Compiler Version Notes

---------------------------------------------
| C               | 619.lbm_s(base, peak) 638.imagick_s(base, peak)  
|                 | 644.nab_s(base, peak) |
---------------------------------------------

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
    Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
---------------------------------------------

---------------------------------------------
| C++, C, Fortran | 607.cactuBSSN_s(base, peak) |
---------------------------------------------

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
    Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
    Version 19.0.4.227 Build 20190416
---------------------------------------------

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)

SPECspeed®2017_fp_base = 132
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CPU2017 License: 9019  Test Date: Aug-2019
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Compiler Version Notes ( Continued )

Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

------------------------------------------------------------------------------
Fortran         | 603.bwaves_s(base, peak) 649.fotonik3d_s(base, peak)
| 654.roms_s(base, peak)
------------------------------------------------------------------------------
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
Fortran, C      | 621.wrf_s(base, peak) 627.cam4_s(base, peak)
| 628.pop2_s(base, peak)
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Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
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Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.4.227 Build 20190416
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 6240M, 2.60GHz)

SPECspeed®2017_fp_base = 132
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Test Sponsor: Cisco Systems
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Base Portability Flags

603.bwaves_s: -DSPEC_LP64  
607.cactuBSSN_s: -DSPEC_LP64  
619.hm_s: -DSPEC_LP64  
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian  
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG  
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian -assume byterecl  
638.imagick_s: -DSPEC_LP64  
644.nab_s: -DSPEC_LP64  
649.fotonik3d_s: -DSPEC_LP64  
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp  
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch  
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-nostandard-realloc-lhs

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

(Continued on next page)
Cisco Systems
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SPEC CPU®2017 Floating Point Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems

SPECspeed®2017_fp_base = 132
SPECspeed®2017_fp_peak = 132

Peak Compiler Invocation (Continued)

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Peak Portability Flags

Same as Base Portability Flags

Peak Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:

603.bwaves_s: -prof-gen(pass 1) -prof-use(pass 2) -DSPEC_SUPPRESS_OPENMP
-DSPEC_OPENMP -O2 -xCORE-AVX512 -qopt-prefetch -ipo -O3
-ffinite-math-only -no-prec-div -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs

649.fotonik3d_s: Same as 603.bwaves_s

654.roms_s: -DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-prefetch -ffinite-math-only -qopt-mem-layout-trans=4
-qopenmp -nostandard-realloc-lhs

Benchmarks using both Fortran and C:

621.wrf_s: -prof-gen(pass 1) -prof-use(pass 2) -O2 -xCORE-AVX512
-qopt-prefetch -ipo -O3 -ffinite-math-only -no-prec-div
-qopt-mem-layout-trans=4 -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

627.cam4_s: -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-DSPEC_OPENMP -nostandard-realloc-lhs

628.pop2_s: Same as 621.wrf_s

(Continued on next page)
### SPEC CPU®2017 Floating Point Speed Result

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**SPECspeed®2017_fp_base = 132**

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</tbody>
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**Peak Optimization Flags (Continued)**

Benchmarks using Fortran, C, and C++:

- xCORE-AVX512
- -ipo
- -O3
- -no-prec-div
- -gopt-prefetch
- -ffinite-math-only
- -gopt-mem-layout-trans=4
- -qopenmp
- -DSPEC_OPENMP
- -nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at:


You can also download the XML flags sources by saving the following links:


---

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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