### SPEC® CPU2017 Floating Point Rate Result

#### Hewlett Packard Enterprise

**Test Sponsor:** HPE  
**Synergy 480 Gen10**  
**CPU2017 License:** 3

<table>
<thead>
<tr>
<th>SPECrate2017_fp_base</th>
<th>118</th>
</tr>
</thead>
</table>

**SPECrate2017_fp_peak:** Not Run

---

**Test Sponsor:** HPE  
**Hardware Availability:** Apr-2019  
**Software Availability:** Feb-2019

**Test Date:** Jul-2019

---

#### Hardware

**CPU Name:** Intel Xeon Silver 4210  
**Max MHz.:** 3200  
**Nominal:** 2200  
**Enabled:** 20 cores, 2 chips, 2 threads/core  
**Orderable:** 1, 2 chip(s)  
**Cache L1:** 32 KB I + 32 KB D on chip per core  
**L2:** 1 MB I+D on chip per core  
**L3:** 13.75 MB I+D on chip per chip  
**Memory:** 384 GB (24 x 16 GB 2Rx8 PC4-2933Y-R, running at 2400)  
**Storage:** 1 x 400 GB SAS SSD, RAID 0  
**Other:** None

---

#### Software

**OS:** SUSE Linux Enterprise Server 15 (x86_64)  
**Kernel:** 4.12.14-23-default  
**Compiler:** C/C++: Version 19.0.2.187 of Intel C/C++  
**Compiler Build:** 20190117 for Linux; Fortran: Version 19.0.2.187 of Intel Fortran  
**Compiler Build:** 20190117 for Linux;  
**Firmware:** HPE BIOS Version I42 05/22/2019 released May-2019  
**File System:** btrfs  
**System State:** Run level 3 (multi-user)  
**Base Pointers:** 64-bit  
**Peak Pointers:** Not Applicable  
**Other:** None

---

**Printed and Distributed by:** Standard Performance Evaluation Corporation (info@spec.org)  
**URL:** https://www.spec.org/
SPEC CPU2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.20 GHz, Intel Xeon Silver 4210)

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

SPECrate2017_fp_base = 118
SPECrate2017_fp_peak = Not Run

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>503.bwaves_r</td>
<td>40</td>
<td>1188</td>
<td>338</td>
<td>1188</td>
<td>338</td>
<td>1188</td>
<td>338</td>
</tr>
<tr>
<td>507.cactuBSSN_r</td>
<td>40</td>
<td>557</td>
<td>90.9</td>
<td>558</td>
<td>90.8</td>
<td>557</td>
<td>90.9</td>
</tr>
<tr>
<td>508.namd_r</td>
<td>40</td>
<td>478</td>
<td>79.5</td>
<td>478</td>
<td>79.5</td>
<td>479</td>
<td>79.4</td>
</tr>
<tr>
<td>510.parest_r</td>
<td>40</td>
<td>1601</td>
<td>65.4</td>
<td>1602</td>
<td>65.3</td>
<td>1617</td>
<td>64.7</td>
</tr>
<tr>
<td>511.povray_r</td>
<td>40</td>
<td>743</td>
<td>126</td>
<td>741</td>
<td>126</td>
<td>747</td>
<td>125</td>
</tr>
<tr>
<td>519.lbm_r</td>
<td>40</td>
<td>527</td>
<td>80.0</td>
<td>529</td>
<td>79.8</td>
<td>528</td>
<td>79.9</td>
</tr>
<tr>
<td>521.wrf_r</td>
<td>40</td>
<td>641</td>
<td>140</td>
<td>632</td>
<td>142</td>
<td>642</td>
<td>140</td>
</tr>
<tr>
<td>526.blender_r</td>
<td>40</td>
<td>525</td>
<td>116</td>
<td>525</td>
<td>116</td>
<td>524</td>
<td>116</td>
</tr>
<tr>
<td>527.cam4_r</td>
<td>40</td>
<td>612</td>
<td>114</td>
<td>621</td>
<td>113</td>
<td>622</td>
<td>112</td>
</tr>
<tr>
<td>538.imagick_r</td>
<td>40</td>
<td>419</td>
<td>238</td>
<td>418</td>
<td>238</td>
<td>415</td>
<td>240</td>
</tr>
<tr>
<td>544.nab_r</td>
<td>40</td>
<td>389</td>
<td>173</td>
<td>390</td>
<td>173</td>
<td>389</td>
<td>173</td>
</tr>
<tr>
<td>549.fotonik3d_r</td>
<td>40</td>
<td>1354</td>
<td>115</td>
<td>1352</td>
<td>115</td>
<td>1357</td>
<td>115</td>
</tr>
<tr>
<td>554.roms_r</td>
<td>40</td>
<td>1059</td>
<td>60.0</td>
<td>1061</td>
<td>59.9</td>
<td>1067</td>
<td>59.6</td>
</tr>
</tbody>
</table>

SPECrate2017_fp_base = 118
SPECrate2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017_u2/lib/ia32:/home/cpu2017_u2/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
SPEC CPU2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.20 GHz, Intel Xeon Silver 4210)

SPECrate2017_fp_base = 118
SPECrate2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License: 3</th>
<th>Test Date: Jul-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: HPE</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: HPE</td>
<td>Software Availability: Feb-2019</td>
</tr>
</tbody>
</table>

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
- Thermal Configuration set to Maximum Cooling
- Memory Patrol Scrubbing set to Disabled
- LLC Prefetch set to Enabled
- LLC Dead Line Allocation set to Disabled
- Enhanced Processor Performance set to Enabled
- Workload Profile set to General Throughput Compute
- Workload Profile set to Custom
- Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017_u2/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on sy480g10-2 Mon Jul 8 23:12:53 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
2 "physical id"s (chips)
40 "processors"
core, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 20
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 2
Core(s) per socket: 10
Socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel

(Continued on next page)
Hewlett Packard Enterprise
Synergy 480 Gen10
(2.20 GHz, Intel Xeon Silver 4210)

SPECrate2017_fp_base = 118
SPECrate2017_fp_peak = Not Run

CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Silver 4210 CPU @ 2.20GHz
Stepping:            6
CPU MHz:             2200.000
BogoMIPS:            4400.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            14080K
NUMA node0 CPU(s):   0-9,20-29
NUMA node1 CPU(s):   10-19,30-39
Flags:               fpu vme de pse sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl apic cpuid
aarch64 cpl3 cmov strcmp stremi smx tm2 tsc pacer msr pae mce cx8
mmx fxsr sse sse2 ssse3 sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_l3 invpcid_single intel_p6 mba tpr_shadow vme tm mmsa vmx
msr pnx saveprix nwmxppcp extable pbe syscall nx pdpe1gb rdtscp
lp64 pid dts dtlbclflush dlbrst dtherm ida arat pfn荥 pkx ospke avx512_vnni
arch_capabilities ssbd

/platforms/cpuinfo_cache_data
    cache size: 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
    available: 2 nodes (0-1)
    node 0 cpus: 0 1 2 3 4 5 6 7 8 9 20 21 22 23 24 25 26 27 28 29
    node 0 size: 193046 MB
    node 0 free: 192504 MB
    node 1 cpus: 10 11 12 13 14 15 16 17 18 19 30 31 32 33 34 35 36 37 38 39
    node 1 size: 193305 MB
    node 1 free: 192983 MB
    node distances:
        node 0 1
        0: 10 21
        1: 21 10

From /proc/meminfo
    MemTotal:      395624552 kB
    HugePages_Total:   0
    Hugepagesize:    2048 kB

(Continued on next page)
Platform Notes (Continued)

From /etc/*release* /etc/*version*

```
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"
```

```
uname -a:
  Linux sy480g10-2 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
  x86_64 x86_64 x86_64 GNU/Linux
```

Kernel self-reported vulnerability status:

- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

```
run-level 3 Jul 8 23:10
```

```
SPEC is set to: /home/cpu2017_u2
  Filesystem   Type Size  Used Avail Use% Mounted on
  /dev/sdb2     btrfs 371G  93G  277G  26% /home
```

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

- BIOS HPE I42 05/22/2019
- Memory:
  24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==============================================================================
CC  519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
------------------------------------------------------------------------------
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
  Version 19.0.2.187 Build 20190117
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

(Continued on next page)
## SPEC CPU2017 Floating Point Rate Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(2.20 GHz, Intel Xeon Silver 4210)  

<table>
<thead>
<tr>
<th>SPECrate2017_fp_base</th>
<th>118</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

- **CPU2017 License:** 3  
- **Test Sponsor:** HPE  
- **Tested by:** HPE  
- **Test Date:** Jul-2019  
- **Hardware Availability:** Apr-2019  
- **Software Availability:** Feb-2019

### Compiler Version Notes (Continued)

```
CXXC 508.namd_r(base) 510.parest_r(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.2.187 Build 20190117 
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

CC 511.povray_r(base) 526.blender_r(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.2.187 Build 20190117 
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

FC 507.cactuBSSN_r(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.2.187 Build 20190117 
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

FC 503.bwaves_r(base) 549.fotonik3d_r(base) 554.roms_r(base)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, 
Version 19.0.2.187 Build 20190117 
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.

CC 521.wrf_r(base) 527.cam4_r(base)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
```

(Continued on next page)
# SPEC CPU2017 Floating Point Rate Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(2.20 GHz, Intel Xeon Silver 4210)  

<table>
<thead>
<tr>
<th>SPECrate2017_fp_base</th>
<th>118</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate2017_fp_peak</td>
<td>Not Run</td>
</tr>
</tbody>
</table>

| CPU2017 License: | 3 |
| Test Sponsor: | HPE |
| Tested by: | HPE |
| Test Date: | Jul-2019 |
| Hardware Availability: | Apr-2019 |
| Software Availability: | Feb-2019 |

## Compiler Version Notes (Continued)

64, Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
Intel (R) C Intel (R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.  
-----------------------------------------------

## Base Compiler Invocation

**C benchmarks:**

```bash
icc -m64 -std=c11
```

**C++ benchmarks:**

```bash
icpc -m64
```

**Fortran benchmarks:**

```bash
ifort -m64
```

**Benchmarks using both Fortran and C:**

```bash
ifort -m64 icc -m64 -std=c11
```

**Benchmarks using both C and C++:**

```bash
icpc -m64 icc -m64 -std=c11
```

**Benchmarks using Fortran, C, and C++:**

```bash
icpc -m64 icc -m64 -std=c11 ifort -m64
```

## Base Portability Flags

- 503.bwaves_r: -DSPEC_LP64
- 507.cactuBSSN_r: -DSPEC_LP64
- 508.namd_r: -DSPEC_LP64
- 510.parest_r: -DSPEC_LP64
- 511.povray_r: -DSPEC_LP64
- 519.lbm_r: -DSPEC_LP64
- 521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
- 526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char
- 527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG
- 538.imagick_r: -DSPEC_LP64
- 544.nab_r: -DSPEC_LP64
- 549.fotonik3d_r: -DSPEC_LP64
- 554.roms_r: -DSPEC_LP64
SPEC CPU2017 Floating Point Rate Result

Hewlett Packard Enterprise
(Test Sponsor: HPE)
Synergy 480 Gen10
(2.20 GHz, Intel Xeon Silver 4210)

SPECrate2017_fp_base = 118
SPECrate2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License: 3</th>
<th>Test Date: Jul-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: HPE</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: HPE</td>
<td>Software Availability: Feb-2019</td>
</tr>
</tbody>
</table>

Base Optimization Flags

C benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

C++ benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Fortran benchmarks:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

Benchmarks using both C and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4

Benchmarks using Fortran, C, and C++:
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs
-align array32byte

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

SPEC is a registered trademark of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-07-09 00:12:53-0400.
Report generated on 2019-08-06 18:00:05 by CPU2017 PDF formatter v6067.
Originally published on 2019-08-06.