## SPEC® CPU2017 Integer Speed Result

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
Synergy 480 Gen10  
(1.90 GHz, Intel Xeon Gold 6262V)  

<table>
<thead>
<tr>
<th>SPECspeed2017_int_base</th>
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<tr>
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| CPU2017 License: | 3 |
| Test Sponsor: | HPE |
| Tested by: | HPE |
| Test Date: | Jul-2019 |
| Hardware Availability: | Apr-2019 |
| Software Availability: | Feb-2019 |

### Hardware

- **CPU Name:** Intel Xeon Gold 6262V  
- **Max MHz.:** 3600  
- **Nominal:** 1900  
- **Enabled:** 48 cores, 2 chips  
- **Orderable:** 1, 2 chip(s)  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **Cache L2:** 1 MB I+D on chip per core  
- **Cache L3:** 33 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (24 x 32 GB 2Rx4 PC4-2933Y-R, running at 2400)  
- **Storage:** 1 x 400 GB SAS SSD, RAID 0  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 15 (x86_64)  
- **Kernel:** 4.12.14-23-default  
- **Compiler:** C/C++: Version 19.0.2.187 of Intel C/C++ Compiler Build 20190117 for Linux; Fortran: Version 19.0.2.187 of Intel Fortran Compiler Build 20190117 for Linux  
- **Parallel:** Yes  
- **Firmware:** HPE BIOS Version I42 04/18/2019 released Apr-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** jemalloc memory allocator V5.0.1

### SPECspeed2017_int_base (9.31)

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Results</th>
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<td>48</td>
<td>6.34</td>
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</table>

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches

General Notes

Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017_u2/lib/ia32:/home/cpu2017_u2/lib/intel64:
/home/cpu2017_u2/je5.0.1-32:/home/cpu2017_u2/je5.0.1-64"
OMP_STACKSIZE = "192M"
Binary compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1)
is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2)
is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation

(Continued on next page)
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SPECspeed2017_int_base = 9.31
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CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

| Test Date: Jul-2019 | Hardware Availability: Apr-2019 | Software Availability: Feb-2019 |

General Notes (Continued)
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

Platform Notes

BIOS Configuration:
Hyper-Threading set to Disabled
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Peak Frequency Compute
Minimum Processor Idle Power Core C-State set to C1E State
Energy/Performance Bias set to Balanced Power
Workload Profile set to Custom
Numa Group Size Optimization set to Flat
Sysinfo program /home/cpu2017_u2/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcede8f2999c33d61f64985e45859ea9
running on sy480-gen10 Sat Jul 6 04:17:59 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6262V CPU @ 1.90GHz
2  "physical id"s (chips)
48 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 24
siblings : 24
physical 0: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29
physical 1: cores 0 1 2 3 4 5 8 9 10 11 12 13 16 17 18 19 20 21 24 25 26 27 28 29

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 48
On-line CPU(s) list: 0-47
Thread(s) per core: 1
Core(s) per socket: 24
Socket(s): 2
NUMA node(s): 2

(Continued on next page)
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Platform Notes (Continued)

Vendor ID:        GenuineIntel
CPU family:       6
Model:            85
Model name:       Intel(R) Xeon(R) Gold 6262V CPU @ 1.90GHz
Stepping:         7
CPU MHz:          1900.000
BogoMIPS:         3800.00
Virtualization:   VT-x
L1d cache:        32K
L1i cache:        32K
L2 cache:         1024K
L3 cache:         33792K
NUMA node0 CPU(s): 0-23
NUMA node1 CPU(s): 24-47
Flags:            fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
                  pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
                  lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
                  aperfmpref tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
                  sdbg fma cx16 xtpr pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt
                  tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
                  epb cat_l3 cdp_l3 invpcid_single intel_ppm mba trp_shadow vmpori ept
                  vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
                  avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
                  xsaveopt xsavec xsaves cqm_llc cqm_occup_llc cqm_mbm_total cqm_mbm_local
                  ibpb ibrs stibp dtherm ida arat pln pts pku ospke avx512_vnni arch_capabilities ssbd

/proc/cpuinfo cache data
  cache size: 33792 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23
  node 0 size: 193016 MB
  node 0 free: 192531 MB
  node 1 cpus: 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
  node 1 size: 193333 MB
  node 1 free: 193041 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 395622536 KB
  HugePages_Total: 0
  Hugepagesize: 2048 KB

(Continued on next page)
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Platform Notes (Continued)

From /etc/*release* /etc/*version*
  os-release:
    NAME="SLES"
    VERSION="15"
    VERSION_ID="15"
    PRETTY_NAME="SUSE Linux Enterprise Server 15"
    ID="sles"
    ID_LIKE="suse"
    ANSI_COLOR="0;32"
    CPE_NAME="cpe:/o:suse:sles:15"

uname -a:
    Linux sy480-gen10 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018 (cd0437b)
    x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:

CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Jul 6 04:16

SPEC is set to: /home/cpu2017_u2
  Filesystem Type Size Used Avail Use% Mounted on
  /dev/sda3 xfs 405G 250G 156G 62% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret
this section. The 'dmidecode' program reads system data which is "intended to allow
hardware to be accurately determined", but the intent may not be met, as there are
frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS HPE I42 04/18/2019
Memory:
  24x UNKNOWN NOT AVAILABLE 16 GB 2 rank 2933, configured at 2400

(End of data from sysinfo program)

Compiler Version Notes

==================================
CC  600.perlbench_s(base) 602.gcc_s(base) 605.mcf_s(base) 625.x264_s(base)
    657.xz_s(base)
==================================

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,

(Continued on next page)
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### Compiler Version Notes (Continued)

```
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
--------------------------------------------------------------------
CXXC 620.omnetpp_s(base) 623.xalancbmk_s(base) 631.deepsjeng_s(base)  
641.leela_s(base)
--------------------------------------------------------------------
```

```
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,  
Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

```
--------------------------------------------------------------------
FC 648.exchange2_s(base)
--------------------------------------------------------------------
```

```
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.2.187 Build 20190117  
Copyright (C) 1985-2019 Intel Corporation. All rights reserved.
```

### Base Compiler Invocation

- **C benchmarks:**  
  icc -m64 -std=c11

- **C++ benchmarks:**  
  icpc -m64

- **Fortran benchmarks:**  
  ifort -m64

### Base Portability Flags

- 600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
- 602.gcc_s: -DSPEC_LP64
- 605.mcf_s: -DSPEC_LP64
- 620.omnetpp_s: -DSPEC_LP64
- 623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
- 625.x264_s: -DSPEC_LP64
- 631.deepsjeng_s: -DSPEC_LP64
- 641.leela_s: -DSPEC_LP64
- 648.exchange2_s: -DSPEC_LP64

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Base Portability Flags (Continued)

657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP  
-L/home/cpu2017_u2/je5.0.1-64/ -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div  
-qopt-mem-layout-trans=4  
-L/usr/local/IntelCompiler19/compilers_and_libraries_2019.1.144/linux/compiler/lib/intel64  
-lqkmalloc

Fortran benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-mem-layout-trans=4  
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.html  
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/HPE-ic19.0u1-flags-linux64.xml  
http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-07-06 05:17:58-0400.  