Hewlett Packard Enterprise
ProLiant DL380 Gen10
(2.80 GHz, Intel Xeon Gold 6242)

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

SPECraten2017_fp_base = 203
SPECraten2017_fp_peak = Not Run

Test Date: May-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

Hardware
CPU Name: Intel Xeon Gold 6242
Max MHz.: 3900
Nominal: 2800
Enabled: 32 cores, 2 chips, 2 threads/core
Orderable: 1, 2 chip(s)
Cache L1: 32 KB I + 32 KB D on chip per core
L2: 1 MB I+D on chip per core
L3: 22 MB I+D on chip per chip
Other: None
Memory: 768 GB (24 x 32 GB 2Rx4 PC4-2933Y-R)
Storage: 1 x 960 GB SATA SSD, RAID 0
Other: None

Software
OS: SUSE Linux Enterprise Server 15 (x86_64)
Kernel 4.12.14-23-default
Compiler: C/C++: Version 19.0.1.144 of Intel C/C++
Compiler Build 20181018 for Linux;
Fortran: Version 19.0.1.144 of Intel Fortran
Compiler Build 20181018 for Linux
Parallel: No
Firmware: HPE BIOS Version U30 04/18/2019 released Apr-2019
File System: btrfs
System State: Run level 3 (multi-user)
Base Pointers: 64-bit
Peak Pointers: Not Applicable
Other: None
SPEC CPU2017 Floating Point Rate Result

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Results Table

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</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3 > /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
umactl --interleave=all runcpu <etc>

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
NA: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10
(2.80 GHz, Intel Xeon Gold 6242)

SPEC CPU2017 Floating Point Rate Result

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SPECrate2017_fp_base = 203
SPECrate2017_fp_peak = Not Run

CPU2017 License: 3
Test Sponsor: HPE
Tested by: HPE

Test Date: May-2019
Hardware Availability: Apr-2019
Software Availability: Nov-2018

General Notes (Continued)

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Platform Notes

BIOS Configuration:
Thermal Configuration set to Maximum Cooling
Memory Patrol Scrubbing set to Disabled
LLC Prefetch set to Enabled
LLC Dead Line Allocation set to Disabled
Enhanced Processor Performance set to Enabled
Workload Profile set to General Throughput Compute
Workload Profile set to Custom
Energy/Performance Bias set to Balanced Performance

Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on dl380-clx-sles15hs Thu May 23 06:52:09 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
2  "physical id"s (chips)
64 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 16
siblings : 32
physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 64
On-line CPU(s) list: 0-63
Thread(s) per core: 2
Core(s) per socket: 16
Socket(s): 2
NUMA node(s): 4
Vendor ID: GenuineIntel

(Continued on next page)
Platform Notes (Continued)

CPU family:          6
Model:               85
Model name:          Intel(R) Xeon(R) Gold 6242 CPU @ 2.80GHz
Stepping:            6
CPU MHz:             2800.000
BogoMIPS:            5600.00
Virtualization:      VT-x
L1d cache:           32K
L1i cache:           32K
L2 cache:            1024K
L3 cache:            22528K
NUMA node0 CPU(s):   0-7,32-39
NUMA node1 CPU(s):   8-15,40-47
NUMA node2 CPU(s):   16-23,48-55
NUMA node3 CPU(s):   24-31,56-63
Flags:               fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid
aperf perfctr tsc_known_freq pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3
sdms fma cx16 xtrr pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt
tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault
epb cat_13 cdp_13 invpcid_single intel_pti mba tpr_shadow vnmi flexpriority ept
vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 erms invpcid rtm cqm mpx rdt_a
avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl
xsaveopt xsaves xsaveas cmcpumlah cqm_occup_llc cqm_mbm_total cqm_mbm_local
ibpb ibrs stib dtherm ida arat pln pts pku ospke avx512_vnni arch_capabilities ssbd

From /proc/cpuinfo cache data

   Proc cache size: 22528 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
   physical chip.

   available: 4 nodes (0-3)
   node 0 cpus: 0 1 2 3 4 5 6 7 32 33 34 35 36 37 38 39
   node 0 size: 193047 MB
   node 0 free: 192441 MB
   node 1 cpus: 8 9 10 11 12 13 14 15 40 41 42 43 44 45 46 47
   node 1 size: 193532 MB
   node 1 free: 193273 MB
   node 2 cpus: 16 17 18 19 20 21 22 23 48 49 50 51 52 53 54 55
   node 2 size: 193532 MB
   node 2 free: 193261 MB
   node 3 cpus: 24 25 26 27 28 29 30 31 56 57 58 59 60 61 62 63
   node 3 size: 193305 MB
   node 3 free: 193131 MB
   node distances:
      node 0 1 2 3

(Continued on next page)
**SPEC CPU2017 Floating Point Rate Result**

**Hewlett Packard Enterprise**  
(Test Sponsor: HPE)  
ProLiant DL380 Gen10  
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<td>Software Availability: Nov-2018</td>
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</table>

**SPECrate2017_fp_base = 203**  
**SPECrate2017_fp_peak = Not Run**

### Platform Notes (Continued)

```plaintext
0: 10 21 31 31  
1: 21 10 31 31  
2: 31 31 10 21  
3: 31 31 21 10
```

From `/proc/meminfo`
- MemTotal: 791981188 kB
- HugePages_Total: 0
- Hugepagesize: 2048 kB

From `/etc/*release* /etc/*version*`
- os-release:
  - NAME="SLES"
  - VERSION="15"
  - VERSION_ID="15"
  - PRETTY_NAME="SUSE Linux Enterprise Server 15"
  - ID="sles"
  - ID_LIKE="suse"
  - ANSI_COLOR="0;32"
  - CPE_NAME="cpe:/o:suse:sles:15"

`uname -a:`
- Linux dl380-clx-sles15hs 4.12.14-23-default #1 SMP Tue May 29 21:04:44 UTC 2018  
  (cd0437b) x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
- CVE-2017-5754 (Meltdown): Not affected
- CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
- CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 May 23 06:49

SPEC is set to: `/home/cpu2017`
- Filesystem Type Size Used Avail Use% Mounted on
  - /dev/sda3 xfs 476G 100G 377G 21% /home

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
- BIOS HPE U30 04/18/2019
- Memory:
  - 24x UNKNOWN NOT AVAILABLE 32 GB 2 rank 2933

(End of data from sysinfo program)
Hewlett Packard Enterprise
(Test Sponsor: HPE)
ProLiant DL380 Gen10
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Test Date: May-2019
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Software Availability: Nov-2018

Compiler Version Notes

==============================================================================
CC 519.lbm_r(base) 538.imagick_r(base) 544.nab_r(base)
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
CXXC 508.namd_r(base) 510.parest_r(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
CC 511.povray_r(base) 526.blender_r(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
FC 507.cactuBSSN_r(base)
Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
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Compiler Version Notes (Continued)

==============================================================================
CC  521.wrf_r(base) 527.cam4_r(base)
Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using both C and C++:
icpc -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

503.bwaves_r: -DSPEC_LP64
507.cactuBSSN_r: -DSPEC_LP64
508.namd_r: -DSPEC_LP64
510.parest_r: -DSPEC_LP64
511.povray_r: -DSPEC_LP64
519.lbm_r: -DSPEC_LP64
521.wrf_r: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
526.blender_r: -DSPEC_LP64 -DSPEC_LINUX -funsigned-char

(Continued on next page)
## SPEC CPU2017 Floating Point Rate Result

**Test Sponsor:** HPE
**ProLiant DL380 Gen10**
*(2.80 GHz, Intel Xeon Gold 6242)*

| SPECrate2017_fp_base = | 203 |
| SPECrate2017_fp_peak = | Not Run |

### Base Portability Flags (Continued)

527.cam4_r: -DSPEC_LP64 -DSPEC_CASE_FLAG  
538.imagick_r: -DSPEC_LP64  
544.nab_r: -DSPEC_LP64  
549.fotonik3d_r: -DSPEC_LP64  
554.roms_r: -DSPEC_LP64

### Base Optimization Flags

**C benchmarks:**  
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4

**C++ benchmarks:**  
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4

**Fortran benchmarks:**  
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

**Benchmarks using both Fortran and C:**  
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

**Benchmarks using both C and C++:**  
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4

**Benchmarks using Fortran, C, and C++:**  
-xCORE-AVX2 -ipo -O3 -no-prec-div -qopt-prefetch -ffinite-math-only  
-qopt-mem-layout-trans=4 -auto -nostandard-realloc-lhs  
-align array32byte

The flags files that were used to format this result can be browsed at:

http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.html

You can also download the XML flags sources by saving the following links:

http://www.spec.org/cpu2017/flags/HPE-Platform-Flags-Intel-V1.2-CLX-revB.xml
### SPEC CPU2017 Floating Point Rate Result

**Hewlett Packard Enterprise**  
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Tested with SPEC CPU2017 v1.0.5 on 2019-05-23 06:52:08-0400.  