### Lenovo Global Technology

**ThinkSystem SR550**  
(2.30 GHz, Intel Xeon Gold 5218)

<table>
<thead>
<tr>
<th>CPU2017 License: 9017</th>
<th>Test Date: Apr-2019</th>
</tr>
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<tbody>
<tr>
<td>Test Sponsor: Lenovo Global Technology</td>
<td>Hardware Availability: Apr-2019</td>
</tr>
<tr>
<td>Tested by: Lenovo Global Technology</td>
<td>Software Availability: Dec-2018</td>
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</tbody>
</table>

**SPECspeed2017_fp_base = 116**  
**SPECspeed2017_fp_peak = Not Run**

### Performance Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed2017_fp_base</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s</td>
<td>32</td>
<td>607.cactuBSSN_s</td>
</tr>
<tr>
<td>619.lbm_s</td>
<td>32</td>
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<tr>
<td>621.wrf_s</td>
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<tr>
<td>627.cam4_s</td>
<td>32</td>
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<tr>
<td>628.pop2_s</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>638.imagick_s</td>
<td>32</td>
<td></td>
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<tr>
<td>644.nab_s</td>
<td>32</td>
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<tr>
<td>649.fotonik3d_s</td>
<td>32</td>
<td></td>
</tr>
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<td>654.roms_s</td>
<td>32</td>
<td></td>
</tr>
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### Hardware

- **CPU Name:** Intel Xeon Gold 5218  
- **Max MHz.:** 3900  
- **Nominal:** 2300  
- **Enabled:** 32 cores, 2 chips  
- **Orderable:** 1.2 chips  
- **Cache L1:** 32 KB I + 32 KB D on chip per core  
- **Cache L2:** 1 MB I-D on chip per core  
- **Cache L3:** 22 MB I+D on chip per chip  
- **Other:** None  
- **Memory:** 384 GB (12 x 32 GB 2Rx4 PC4-2933Y-R, running at 2666)  
- **Storage:** 1 x 960 GB SATA SSD  
- **Other:** None

### Software

- **OS:** SUSE Linux Enterprise Server 12 SP4 (x86_64)  
- **Kernel:** 4.12.14-94.41-default  
- **Compiler:** C/C++: Version 19.0.1.144 of Intel C/C++ Compiler Build 20181018 for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler Build 20181018 for Linux  
- **Parallel:** Yes  
- **Firmware:** Lenovo BIOS Version TEE135L 2.10 released Jan-2019  
- **File System:** xfs  
- **System State:** Run level 3 (multi-user)  
- **Base Pointers:** 64-bit  
- **Peak Pointers:** Not Applicable  
- **Other:** None
Lenovo Global Technology
ThinkSystem SR550
(2.30 GHz, Intel Xeon Gold 5218)

CPU2017 License: 9017
Test Sponsor: Lenovo Global Technology
Tested by: Lenovo Global Technology

SPECspeed2017_fp_base = 116
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Results Table

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<tr>
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<th>Threads</th>
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<th>Ratio</th>
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</tbody>
</table>

SPECspeed2017_fp_base = 116
SPECspeed2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

General Notes
Environment variables set by runcpu before the start of the run:
KMP_AFFINITY = "granularity=fine,compact"
LD_LIBRARY_PATH = "/home/cpu2017-1.0.5-ic19.0u1/lib/intel64"
OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.5
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
 sync; echo 3> /proc/sys/vm/drop_caches
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3640 (Spectre variant 3a) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2018-3639 (Spectre variant 4) is mitigated in the system as tested and documented.
Platform Notes

BIOS configuration:
Choose Operating Mode set to Maximum Performance
Choose Operating Mode set to Custom Mode
MONITOR/MWAIT set to Enable
Hyper-Threading set to Disable
Sysinfo program /home/cpu2017-1.0.5-ic19.0u1/bin/sysinfo
Rev: r5974 of 2018-05-19 9bcde8f2999c33d61f64985e45859ea9
running on linux-dogi Thu Apr 11 08:21:52 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
  model name : Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
  2  "physical id"s (chips)
  32 "processors"
  cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
    cpu cores : 16
    siblings : 16
    physical 0: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
    physical 1: cores 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

From lscpu:
  Architecture:          x86_64
  CPU op-mode(s):        32-bit, 64-bit
  Byte Order:            Little Endian
  CPU(s):                32
  On-line CPU(s) list:   0-31
  Thread(s) per core:    1
  Core(s) per socket:    16
  Socket(s):             2
  NUMA node(s):          2
  Vendor ID:             GenuineIntel
  CPU family:            6
  Model:                 85
  Model name:            Intel(R) Xeon(R) Gold 5218 CPU @ 2.30GHz
  Stepping:              6
  CPU MHz:               2300.000
  CPU max MHz:           3900.0000
  CPU min MHz:           1000.0000
  BogoMIPS:              4600.00
  Virtualization:        VT-x
  L1d cache:             32K
  L1i cache:             32K
  L2 cache:              1024K

(Continued on next page)
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**Platform Notes (Continued)**

L3 cache: 22528K  
NUMA node0 CPU(s): 0-15  
NUMA node1 CPU(s): 16-31  
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp lm constant_tsc art arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc cpuid aperfmperf pnpi pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg fma cx16 xtrunc pdcm pcid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes xsave avx f16c rdrand lahf_lm abm 3dnowprefetch cpuid_fault epb cat_l3 cdp_l3 invpcid_single ssbd mba ibrs ibp stibp tpr_shadow vmmi flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle avx2 smep bmi2 ertms invpcid rtm cmq mpx rdt_a avx512f avx512dq rdseed adx smap clflushopt clwb intel_pt avx512cd avx512bw avx512vl xsaveopt xsaves cqm_llc cqm_occup_llc cqm_mbb_total cqm_mbb_local dtherm ida arat pln pts pkup ospke avx512_vnni flush_lld arch_capabilities

/proc/cpuinfo cache data  

```plaintext  
  cache size: 22528 KB  
```

From numactl --hardware  
WARNING: a numactl 'node' might or might not correspond to a physical chip.  
  available: 2 nodes (0-1)  
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15  
  node 0 size: 193125 MB  
  node 0 free: 192698 MB  
  node 1 cpus: 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31  
  node 1 size: 193480 MB  
  node 1 free: 192897 MB  
  node distances:  
  node 0 1  
  0: 10 21  
  1: 21 10  

From /proc/meminfo  
MemTotal: 395884500 kB  
HugePages_Total: 0  
Hugepagesize: 2048 kB  

From /etc/*release*/etc/*version*  
SuSE-release:  
  SUSE Linux Enterprise Server 12 (x86_64)  
  VERSION = 12  
  PATCHLEVEL = 4  
  # This file is deprecated and will be removed in a future service pack or release.  
  # Please check /etc/os-release for details about this release.  
  os-release:  
  NAME="SLES"  
  VERSION="12-SP4"  

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(Continued on next page)
SPEC CPU2017 Floating Point Speed Result

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Platform Notes (Continued)

VERSION_ID="12.4"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP4"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp4"

uname -a:
x86_64 x86_64 x86_64 GNU/Linux

Kernel self-reported vulnerability status:
CVE-2017-5754 (Meltdown): Not affected
CVE-2017-5753 (Spectre variant 1): Mitigation: __user pointer sanitization
CVE-2017-5715 (Spectre variant 2): Mitigation: Indirect Branch Restricted Speculation, IBPB, IBRS_FW

run-level 3 Apr 11 08:20

SPEC is set to: /home/cpu2017-1.0.5-ic19.0u1
    Filesystem Type Size Used Avail Use% Mounted on
    /dev/sda3 xfs 892G 40G 852G 5% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.
    BIOS Lenovo -[TEE135L-2.10]- 01/10/2019
    Memory:
      12x SK Hynix HMA84GR7CJR4N-WM 32 GB 2 rank 2933, configured at 2666

(End of data from sysinfo program)

Compiler Version Notes
==============================================================================
CC  619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
==============================================================================
Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
==============================================================================
FC  607.cactuBSSN_s(base)
==============================================================================

(Continued on next page)
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**Compiler Version Notes (Continued)**

Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64,
Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R)
64, Version 19.0.1.144 Build 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

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**Base Compiler Invocation**

**C benchmarks:**
icc -m64 -std=c11

**Fortran benchmarks:**
ifort -m64

**Benchmarks using both Fortran and C:**
ifort -m64 icc -m64 -std=c11

**Benchmarks using Fortran, C, and C++:**
icpc -m64 icc -m64 -std=c11 ifort -m64
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Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactuBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp
-nostandard-realloc-lhs

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=4 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs

The flags files that were used to format this result can be browsed at
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-A.html

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Lenovo-Platform-SPECcpu2017-Flags-V1.2-CLX-A.xml
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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU2017 v1.0.5 on 2019-04-10 20:21:51-0400.