# SPEC CPU® 2017 Integer Speed Result

## Cisco Systems

Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

<table>
<thead>
<tr>
<th>Software</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_base</td>
<td>7.64</td>
</tr>
<tr>
<td>SPECspeed®2017_int_peak</td>
<td>7.89</td>
</tr>
</tbody>
</table>

## Test Results

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>SPECspeed®2017_int_base</th>
<th>SPECspeed®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>perlbench_s</td>
<td>40</td>
<td>6.36</td>
<td>7.89</td>
</tr>
<tr>
<td>gcc_s</td>
<td>40</td>
<td>6.05</td>
<td>9.71</td>
</tr>
<tr>
<td>mcf_s</td>
<td>40</td>
<td>4.49</td>
<td>7.98</td>
</tr>
<tr>
<td>omnetpp_s</td>
<td>40</td>
<td>8.23</td>
<td>9.85</td>
</tr>
<tr>
<td>xalanchmk_s</td>
<td>40</td>
<td>8.79</td>
<td>9.85</td>
</tr>
<tr>
<td>x264_s</td>
<td>40</td>
<td>11.2</td>
<td>12.8</td>
</tr>
<tr>
<td>deepsjeng_s</td>
<td>40</td>
<td>9.44</td>
<td>11.6</td>
</tr>
<tr>
<td>leela_s</td>
<td>40</td>
<td>12.8</td>
<td>15.0</td>
</tr>
<tr>
<td>exchange2_s</td>
<td>40</td>
<td>13.8</td>
<td>19.5</td>
</tr>
<tr>
<td>xz_s</td>
<td>40</td>
<td>19.2</td>
<td>19.5</td>
</tr>
</tbody>
</table>

## Hardware

- **CPU Name:** Intel Xeon Gold 5115
- **Max MHz:** 3200
- **Nominal:** 2400
- **Enabled:** 40 cores, 4 chips
- **Orderable:** 2,4 Chips
- **Cache L1:** 32 KB I + 32 KB D on chip per core
- **L2:** 1 MB I+D on chip per core
- **L3:** 13.75 MB I+D on chip per chip
- **Other:** None
- **Memory:** 1536 GB (48 x 32 GB 2Rx4 PC4-2666V-R, running at 2400)
- **Storage:** 1 x 1 TB HDD, 7.2K RPM
- **Other:** None
- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **Compiler:** C/C++: Version 19.0.0.117 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.0.117 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.1.3e released Jun-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --

## Software

- **OS:** SUSE Linux Enterprise Server 12 SP2 (x86_64)
- **Compiler:** C/C++: Version 19.0.0.117 of Intel C/C++ Compiler for Linux;
  Fortran: Version 19.0.0.117 of Intel Fortran Compiler for Linux
- **Parallel:** Yes
- **Firmware:** Version 3.1.3e released Jun-2018
- **File System:** xfs
- **System State:** Run level 3 (multi-user)
- **Base Pointers:** 64-bit
- **Peak Pointers:** 32/64-bit
- **Other:** jemalloc memory allocator V5.0.1
- **Power Management:** --
**SPEC CPU®2017 Integer Speed Result**

**Cisco Systems**
Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

<table>
<thead>
<tr>
<th>Copyright 2017-2020 Standard Performance Evaluation Corporation</th>
</tr>
</thead>
</table>

**SPECspeed®2017_int_base = 7.64**
**SPECspeed®2017_int_peak = 7.89**

<table>
<thead>
<tr>
<th>CPU2017 License: 9019</th>
<th>Test Date: Feb-2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor: Cisco Systems</td>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Tested by: Cisco Systems</td>
<td>Software Availability: Oct-2018</td>
</tr>
</tbody>
</table>

---

## Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>SPECspeed®2017_int_base = 7.64</th>
<th>SPECspeed®2017_int_peak = 7.89</th>
</tr>
</thead>
<tbody>
<tr>
<td>600.perlbench_s</td>
<td>40</td>
<td>331</td>
<td>5.37</td>
<td>331</td>
<td>5.36</td>
<td>332</td>
<td>5.35</td>
<td>40</td>
<td>281</td>
<td>6.33</td>
<td>278</td>
<td>6.39</td>
<td>279</td>
<td>6.36</td>
<td>7.64</td>
<td>7.89</td>
</tr>
<tr>
<td>602.gcc_s</td>
<td>40</td>
<td>502</td>
<td>7.94</td>
<td>505</td>
<td>7.88</td>
<td>506</td>
<td>7.87</td>
<td>40</td>
<td>494</td>
<td>8.07</td>
<td>496</td>
<td>8.03</td>
<td>495</td>
<td>8.05</td>
<td>7.89</td>
<td>7.89</td>
</tr>
<tr>
<td>605.mcf_s</td>
<td>40</td>
<td>490</td>
<td>9.64</td>
<td>486</td>
<td>9.71</td>
<td>485</td>
<td>9.73</td>
<td>40</td>
<td>483</td>
<td>9.77</td>
<td>479</td>
<td>9.85</td>
<td>479</td>
<td>9.85</td>
<td>7.64</td>
<td>7.89</td>
</tr>
<tr>
<td>620.omnetpp_s</td>
<td>40</td>
<td>363</td>
<td>4.49</td>
<td>365</td>
<td>4.46</td>
<td>354</td>
<td>4.60</td>
<td>40</td>
<td>338</td>
<td>4.82</td>
<td>357</td>
<td>4.57</td>
<td>341</td>
<td>4.79</td>
<td>7.64</td>
<td>7.89</td>
</tr>
<tr>
<td>623.xalanchmk_s</td>
<td>40</td>
<td>172</td>
<td>8.23</td>
<td>173</td>
<td>8.20</td>
<td>172</td>
<td>8.23</td>
<td>40</td>
<td>162</td>
<td>8.77</td>
<td>161</td>
<td>8.79</td>
<td>160</td>
<td>8.85</td>
<td>7.64</td>
<td>7.89</td>
</tr>
<tr>
<td>625.x264_s</td>
<td>40</td>
<td>158</td>
<td>11.1</td>
<td>159</td>
<td>11.1</td>
<td>158</td>
<td>11.2</td>
<td>40</td>
<td>158</td>
<td>11.1</td>
<td>158</td>
<td>11.2</td>
<td>158</td>
<td>11.1</td>
<td>7.64</td>
<td>7.89</td>
</tr>
<tr>
<td>631.deepsjeng_s</td>
<td>40</td>
<td>438</td>
<td>3.90</td>
<td>438</td>
<td>3.90</td>
<td>438</td>
<td>3.89</td>
<td>40</td>
<td>441</td>
<td>3.87</td>
<td>441</td>
<td>3.87</td>
<td>441</td>
<td>3.87</td>
<td>7.64</td>
<td>7.89</td>
</tr>
<tr>
<td>641.leela_s</td>
<td>40</td>
<td>253</td>
<td>11.6</td>
<td>254</td>
<td>11.6</td>
<td>253</td>
<td>11.6</td>
<td>40</td>
<td>252</td>
<td>11.6</td>
<td>253</td>
<td>11.6</td>
<td>253</td>
<td>11.6</td>
<td>7.64</td>
<td>7.89</td>
</tr>
<tr>
<td>657.xz_s</td>
<td>40</td>
<td>316</td>
<td>19.6</td>
<td>319</td>
<td>19.4</td>
<td>317</td>
<td>19.5</td>
<td>40</td>
<td>314</td>
<td>19.7</td>
<td>314</td>
<td>19.7</td>
<td>312</td>
<td>19.8</td>
<td>7.64</td>
<td>7.89</td>
</tr>
</tbody>
</table>

---

### Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,scatter"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i9-7900X CPU + 32GB RAM memory using Redhat Enterprise Linux 7.5

Transparent Huge Pages enabled by default

Prior to runcpu invocation

Filesystem page cache synced and cleared with:
```
sync; echo 3> /proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

SPECspeed\textsuperscript{\textregistered}2017\textunderscore int\textunderscore peak = 7.89
SPECspeed\textsuperscript{\textregistered}2017\textunderscore int\textunderscore base = 7.64

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2019
Hardware Availability: Aug-2017
Software Availability: Oct-2018

BIOS Settings:
Intel HyperThreading Technology set to Disabled
CPU performance set to Enterprise
Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd61b05c091c0f
running on linux-e8np Mon Feb 18 01:09:49 2019

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz
  4 "physical id"s (chips)
  40 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
 excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 10
siblings : 10
physical 0: cores 0 1 2 3 4 8 9 10 11 12
physical 1: cores 0 1 2 3 4 8 9 10 11 12
physical 2: cores 0 1 2 3 4 8 9 10 11 12
physical 3: cores 0 1 2 3 4 8 9 10 11 12

From lscpu:
Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 40
On-line CPU(s) list: 0-39
Thread(s) per core: 1
Core(s) per socket: 10
Socket(s): 4
NUMA node(s): 4
Vendor ID: GenuineIntel
CPU family: 6
Model: 85
Model name: Intel(R) Xeon(R) Gold 5115 CPU @ 2.40GHz
Stepping: 4
CPU MHz: 1721.529
CPU max MHz: 3200.0000
CPU min MHz: 1000.0000
BogoMIPS: 4794.87
Virtualization: VT-x

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems
Test Date: Feb-2019
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Platform Notes (Continued)

L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 14080K
NUMA node0 CPU(s): 0-9
NUMA node1 CPU(s): 10-19
NUMA node2 CPU(s): 20-29
NUMA node3 CPU(s): 30-39
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good nopl apic nonstop_tsc
aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtrp pdcn pccid dis se4_1 ss4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwp_act_window hwp_epp hwp próprio intel_pt rsb_ctxsw spec_ctrl sibp
dretbin kaiser tpr_shadow vnmi flexpriority emt64 fsal fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 ertms invpd rtm cmp mmx avx512f avx512dq rdseed adx smap clflushopt
clwb avx512cd avx512bw avx512vl xsaveopt xsavec xsave vcq_mla vcq_marc vcq_mcc

/proc/cpuinfo cache data
  cache size : 14080 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a physical chip.
  available: 4 nodes (0-3)
  node 0 cpus: 0 1 2 3 4 5 6 7 8 9
  node 0 size: 385623 MB
  node 0 free: 385425 MB
  node 1 cpus: 10 11 12 13 14 15 16 17 18 19
  node 1 size: 387057 MB
  node 1 free: 386810 MB
  node 2 cpus: 20 21 22 23 24 25 26 27 28 29
  node 2 size: 387057 MB
  node 2 free: 386858 MB
  node 3 cpus: 30 31 32 33 34 35 36 37 38 39
  node 3 size: 387054 MB
  node 3 free: 386709 MB
  node distances:
    node 0 1 2 3
      0: 10 21 21 31
      1: 21 10 31 21
      2: 21 31 10 21
      3: 31 21 21 10

From /proc/meminfo
  MemTotal: 1583915688 kB
  HugePages_Total: 0

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

**SPEC CPU®2017 Integer Speed Result**

<table>
<thead>
<tr>
<th>SPECspeed®2017_int_base = 7.64</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECspeed®2017_int_peak = 7.89</td>
</tr>
</tbody>
</table>

---

**Platform Notes (Continued)**

Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*:
SuSE-release:

SUSE Linux Enterprise Server 12 (x86_64)
VERSION = 12
PATCHLEVEL = 2

# This file is deprecated and will be removed in a future service pack or release.
# Please check /etc/os-release for details about this release.

os-release:
NAME="SLES"
VERSION="12-SP2"
VERSION_ID="12.2"
PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
ID="sles"
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
Linux linux-e8np 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Feb 18 00:55

SPEC is set to: /home/cpu2017

Filesystem Type Size Used Avail Use% Mounted on
/dev/sda1 xfs 894G 166G 729G 19% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C480M5.3.1.3e.0.0613081801 06/13/2018
Memory:
48x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666, configured at 2400

(End of data from sysinfo program)

---

**Compiler Version Notes**

<table>
<thead>
<tr>
<th>C</th>
<th>600.perlbench_s(base, peak) 602.gcc_s(base, peak) 605.mcf_s(base, peak) 625.x264_s(base, peak) 657.xz_s(base, peak)</th>
</tr>
</thead>
</table>

Intel(R) C Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804

(Continued on next page)
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

| SPECspeed®2017_int_base = 7.64 |
| SPECspeed®2017_int_peak = 7.89 |

| CPU2017 License: 9019 | Test Date: Feb-2019 |
| Test Sponsor: Cisco Systems | Hardware Availability: Aug-2017 |
| Tested by: Cisco Systems | Software Availability: Oct-2018 |

**Compiler Version Notes (Continued)**

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

<table>
<thead>
<tr>
<th>Compiler Version Notes (Continued)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C++</td>
</tr>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.0.117 Build 20180804</td>
</tr>
<tr>
<td>Copyright (C) 1985-2018 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>C++</td>
</tr>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804</td>
</tr>
<tr>
<td>Copyright (C) 1985-2018 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>C++</td>
</tr>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on IA-32, Version 19.0.0.117 Build 20180804</td>
</tr>
<tr>
<td>Copyright (C) 1985-2018 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>C++</td>
</tr>
<tr>
<td>Intel(R) C++ Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804</td>
</tr>
<tr>
<td>Copyright (C) 1985-2018 Intel Corporation. All rights reserved.</td>
</tr>
<tr>
<td>Fortran</td>
</tr>
<tr>
<td>Intel(R) Fortran Intel(R) 64 Compiler for applications running on Intel(R) 64, Version 19.0.0.117 Build 20180804</td>
</tr>
<tr>
<td>Copyright (C) 1985-2018 Intel Corporation. All rights reserved.</td>
</tr>
</tbody>
</table>
Cisco Systems  Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

SPEC®2017_int_base = 7.64
SPEC®2017_int_peak = 7.89

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Feb-2019
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -DSPEC_LP64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Base Optimization Flags

C benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

C++ benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/usr/local/je5.0.1-64/lib -ljemalloc

Fortran benchmarks:
-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

SPEC CPU®2017 Integer Speed Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

SPECspeed®2017_int_base = 7.64
SPECspeed®2017_int_peak = 7.89

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Feb-2019
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Peak Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks (except as noted below):
icpc -m64

623.xalancbmk_s: icpc -m32 -L/usr/local/IntelCompiler19/compilers_and_libraries_2019.0.117/linux/compiler/lib/ia32_lin

Fortran benchmarks:
ifort -m64

Peak Portability Flags

600.perlbench_s: -DSPEC_LP64 -DSPEC_LINUX_X64
602.gcc_s: -DSPEC_LP64
605.mcf_s: -DSPEC_LP64
620.omnetpp_s: -DSPEC_LP64
623.xalancbmk_s: -D_FILE_OFFSET_BITS=64 -DSPEC_LINUX
625.x264_s: -DSPEC_LP64
631.deepsjeng_s: -DSPEC_LP64
641.leela_s: -DSPEC_LP64
648.exchange2_s: -DSPEC_LP64
657.xz_s: -DSPEC_LP64

Peak Optimization Flags

C benchmarks:
600.perlbench_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -fno-strict-overflow
-L/usr/local/jes5.0.1-64/lib -ljemalloc

602.gcc_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -O2
-xCORE-AVX512 -qopt-mem-layout-trans=3 -ipo -O3
-no-prec-div -DSPEC_SUPPRESS_OPENMP -qopenmp
-DSPEC_OPENMP -L/usr/local/jes5.0.1-64/lib -ljemalloc

605.mcf_s: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -qopenmp -DSPEC_OPENMP
Cisco Systems
Cisco UCS C480 M5 (Intel Xeon Gold 5115, 2.40 GHz)

SPECspeed®2017_int_base = 7.64
SPECspeed®2017_int_peak = 7.89

CPU2017 License: 9019
Test Date: Feb-2019
Test Sponsor: Cisco Systems
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Oct-2018

Peak Optimization Flags (Continued)

605.mcf_s (continued):
-L/usr/local/je5.0.1-64/lib -ljemalloc

625.x264_s: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

657.xz_s: Same as 602.gcc_s

C++ benchmarks:

620.omnetpp_s: -Wl,-z,muldefs -prof-gen(pass1) -prof-use(pass2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

623.xalancbmk_s: -Wl,-z,muldefs -prof-gen(pass1) -prof-use(pass2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-DSPEC_SUPPRESS_OPENMP -gopenmp -DSPEC_OPENMP
-L/usr/local/je5.0.1-64/lib -ljemalloc

631.deepsjeng_s: Same as 620.omnetpp_s

641.leela_s: Same as 620.omnetpp_s

Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/usr/local/je5.0.1-64/lib -ljemalloc

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

SPEC CPU and SPECspeed are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2019-02-18 01:09:49-0500.
Report generated on 2020-07-01 14:38:30 by CPU2017 PDF formatter v6255.
Originally published on 2019-03-05.