# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

<table>
<thead>
<tr>
<th>Copies</th>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>32.7</td>
<td>32.0</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>36.5</td>
<td>38.5</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>23.7</td>
<td>24.2</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>34.8</td>
<td>39.0</td>
</tr>
<tr>
<td>523.xalancbmk_r</td>
<td>59.6</td>
<td>61.8</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>29.2</td>
<td>28.9</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>24.2</td>
<td>24.0</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>21.7</td>
<td>21.7</td>
</tr>
</tbody>
</table>

## Hardware

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU Name</td>
<td>Intel Xeon Bronze 3104</td>
</tr>
<tr>
<td>Max MHz</td>
<td>1700</td>
</tr>
<tr>
<td>Nominal</td>
<td>1700</td>
</tr>
<tr>
<td>Enabled</td>
<td>12 cores, 2 chips</td>
</tr>
<tr>
<td>Orderable</td>
<td>1.2 Chips</td>
</tr>
<tr>
<td>Cache L1</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3</td>
<td>8.25 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
<tr>
<td>Memory</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2666V-R, running at 2133)</td>
</tr>
<tr>
<td>Storage</td>
<td>1 x 600G SAS 10K RPM</td>
</tr>
<tr>
<td>Other</td>
<td>None</td>
</tr>
</tbody>
</table>

## Software

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>OS</td>
<td>SUSE Linux Enterprise Server 12 SP2 (x86_64) 4.4.120-92.70-default</td>
</tr>
<tr>
<td>Compiler</td>
<td>C/C++: Version 19.0.1.144 of Intel C/C++ Compiler for Linux; Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux</td>
</tr>
<tr>
<td>Parallel</td>
<td>No</td>
</tr>
<tr>
<td>Firmware</td>
<td>Version 4.0.1 released Oct-2018</td>
</tr>
<tr>
<td>File System</td>
<td>xfs</td>
</tr>
<tr>
<td>System State</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers</td>
<td>32/64-bit</td>
</tr>
<tr>
<td>Other</td>
<td>jemalloc memory allocator V5.0.1</td>
</tr>
<tr>
<td>Power Management</td>
<td>--</td>
</tr>
</tbody>
</table>

## Test Information

- **CPU2017 License**: 9019
- **Test Sponsor**: Cisco Systems
- **Test Date**: Dec-2018
- **Hardware Availability**: Aug-2017
- **Software Availability**: Oct-2018
- **Tested by**: Cisco Systems

---

By [Standard Performance Evaluation Corporation](https://www.spec.org)
Cisco Systems

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Results Table

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Copies</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>500.perlbench_r</td>
<td>12</td>
<td>670</td>
<td>28.5</td>
<td>671</td>
<td>28.5</td>
<td>667</td>
<td>28.6</td>
<td>12</td>
<td>587</td>
<td>32.5</td>
<td>584</td>
<td>32.7</td>
<td>585</td>
</tr>
<tr>
<td>502.gcc_r</td>
<td>12</td>
<td>531</td>
<td>32.0</td>
<td>531</td>
<td>32.0</td>
<td>532</td>
<td>31.9</td>
<td>12</td>
<td>465</td>
<td>36.5</td>
<td>465</td>
<td>36.5</td>
<td>465</td>
</tr>
<tr>
<td>505.mcf_r</td>
<td>12</td>
<td>504</td>
<td>38.5</td>
<td>504</td>
<td>38.5</td>
<td>504</td>
<td>38.5</td>
<td>12</td>
<td>504</td>
<td>38.5</td>
<td>504</td>
<td>38.5</td>
<td>504</td>
</tr>
<tr>
<td>520.omnetpp_r</td>
<td>12</td>
<td>666</td>
<td>23.6</td>
<td>662</td>
<td>23.8</td>
<td>665</td>
<td>23.7</td>
<td>12</td>
<td>652</td>
<td>24.1</td>
<td>651</td>
<td>24.2</td>
<td>652</td>
</tr>
<tr>
<td>523.xalanbk_r</td>
<td>12</td>
<td>366</td>
<td>34.6</td>
<td>364</td>
<td>34.8</td>
<td>363</td>
<td>34.9</td>
<td>12</td>
<td>326</td>
<td>38.9</td>
<td>325</td>
<td>39.0</td>
<td>325</td>
</tr>
<tr>
<td>525.x264_r</td>
<td>12</td>
<td>352</td>
<td>59.6</td>
<td>352</td>
<td>59.6</td>
<td>352</td>
<td>59.7</td>
<td>12</td>
<td>340</td>
<td>61.8</td>
<td>340</td>
<td>61.8</td>
<td>340</td>
</tr>
<tr>
<td>531.deepsjeng_r</td>
<td>12</td>
<td>471</td>
<td>29.2</td>
<td>471</td>
<td>29.2</td>
<td>471</td>
<td>29.2</td>
<td>12</td>
<td>477</td>
<td>28.9</td>
<td>477</td>
<td>28.8</td>
<td>476</td>
</tr>
<tr>
<td>541.leela_r</td>
<td>12</td>
<td>823</td>
<td>24.2</td>
<td>822</td>
<td>24.2</td>
<td>822</td>
<td>24.2</td>
<td>12</td>
<td>829</td>
<td>24.0</td>
<td>828</td>
<td>24.0</td>
<td>829</td>
</tr>
<tr>
<td>548.exchange2_r</td>
<td>12</td>
<td>479</td>
<td>65.6</td>
<td>480</td>
<td>65.5</td>
<td>481</td>
<td>65.4</td>
<td>12</td>
<td>478</td>
<td>65.7</td>
<td>477</td>
<td>65.9</td>
<td>478</td>
</tr>
<tr>
<td>557.xz_r</td>
<td>12</td>
<td>598</td>
<td>21.7</td>
<td>598</td>
<td>21.7</td>
<td>598</td>
<td>21.7</td>
<td>12</td>
<td>598</td>
<td>21.7</td>
<td>598</td>
<td>21.7</td>
<td>598</td>
</tr>
</tbody>
</table>

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

Submit Notes

The numactl mechanism was used to bind copies to processors. The config file option 'submit' was used to generate numactl commands to bind each copy to a specific processor. For details, please see the config file.

Operating System Notes

Stack size set to unlimited using "ulimit -s unlimited"

General Notes

Environment variables set by runcpu before the start of the run:
LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:
sync; echo 3> /proc/sys/vm/drop_caches
runcpu command invoked through numactl i.e.:
numactl --interleave=all runcpu <etc>
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

**SPEC CPU®2017 Integer Rate Result**

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Test Date:</td>
<td>Dec-2018</td>
</tr>
<tr>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Software Availability:</td>
<td>Oct-2018</td>
</tr>
</tbody>
</table>

**General Notes (Continued)**

is mitigated in the system as tested and documented.
jemalloc, a general purpose malloc implementation
built with the RedHat Enterprise 7.5, and the system compiler gcc 4.8.5

**Platform Notes**

BIOS Settings:

- CPU performance set to Enterprise
- Power Performance Tuning set to OS Controls
- SNC set to Enabled
- IMC Interleaving set to 1-way Interleave
- Patrol Scrub set to Disabled
- Sysinfo program /home/cpu2017/bin/sysinfo
- Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618bcc091c0f
- running on linux-fdny Thu Dec 13 08:12:21 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
https://www.spec.org/cpu2017/Docs/config.html#sysinfo

From /proc/cpuinfo

- model name: Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
- 2 "physical id"s (chips)
- 12 "processors"
- cores, siblings (Caution: counting these is hw and system dependent. The following excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
- cpu cores: 6
- siblings: 6
- physical 0: cores 0 1 2 3 4 5
- physical 1: cores 0 1 2 3 4 5

From lscpu:

- Architecture: x86_64
- CPU op-mode(s): 32-bit, 64-bit
- Byte Order: Little Endian
- CPU(s): 12
- On-line CPU(s) list: 0-11
- Thread(s) per core: 1
- Core(s) per socket: 6
- Socket(s): 2
- NUMA node(s): 2
- Vendor ID: GenuineIntel
- CPU family: 6
- Model: 85

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPECrate®2017_int_base = 33.4
SPECrate®2017_int_peak = 34.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2018
Hardware Availability: Aug-2017
Tested by: Cisco Systems
Software Availability: Oct-2018

Platform Notes (Continued)

Model name: Intel(R) Xeon(R) Bronze 3104 CPU @ 1.70GHz
Stepping: 4
CPU MHz: 1655.500
CPU max MHz: 1700.0000
CPU min MHz: 800.0000
BogoMIPS: 3392.02
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 1024K
L3 cache: 8448K
NUMA node0 CPU(s): 0-5
NUMA node1 CPU(s): 6-11
Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good ntopperf perf jf mce pbe syscall nx pge mca
cmov pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc art arch_perfmon pebs bts rep_good ntopperf perf jf mce pbe syscall nx pge mca
cmov

/proc/cpuinfo cache data
  cache size : 8448 KB

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.
  available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3 4 5
  node 0 free: 386570 MB
  node 1 cpus: 6 7 8 9 10 11
  node 1 free: 387054 MB
  node distances:
    node 0 1
    0: 10 21
    1: 21 10

From /proc/meminfo
  MemTotal: 792192360 kB
  HugePages_Total: 0
  Hugepagesize: 2048 kB

From /etc/*release* /etc/*version*

(Continued on next page)
# SPEC CPU®2017 Integer Rate Result

## Cisco Systems

Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base</th>
<th>SPECrate®2017_int_peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>33.4</td>
<td>34.8</td>
</tr>
</tbody>
</table>

**CPU2017 License:** 9019

**Test Date:** Dec-2018

**Test Sponsor:** Cisco Systems

**Tested by:** Cisco Systems

### Platform Notes (Continued)

SuSE-release:

- SUSE Linux Enterprise Server 12 (x86_64)
- VERSION = 12
- PATCHLEVEL = 2

# This file is deprecated and will be removed in a future service pack or release.

# Please check /etc/os-release for details about this release.

os-release:

- NAME="SLES"
- VERSION="12-SP2"
- VERSION_ID="12.2"
- PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
- ID="sles"
- ANSI_COLOR="0;32"
- CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:

```
Linux linux-fdny 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de) x86_64 x86_64 x86_64 GNU/Linux
```

run-level 3 Dec 13 01:46

SPEC is set to: /home/cpu2017

### Compiler Version Notes

```
C | 500.perlbench_r(base, peak) 502.gcc_r(base, peak) 505.mcf_r(base, peak) 525.x264_r(base, peak) 557.xz_r(base, peak)
```

**icc (ICC) 19.0.1.144 20181018**

Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPEC CPU®2017 Integer Rate Result

SPECrat®2017_int_base = 33.4
SPECrat®2017_int_peak = 34.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Compiler Version Notes (Continued)

C++
520.omnetpp_r(base, peak) 523.xalancbm_r(base, peak)
      531.deepsjeng_r(base, peak) 541.leela_r(base, peak)

------------------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------
==============================================================================
Fortran
548.exchange2_r(base, peak)
------------------------------------------------------------------------------
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

C++ benchmarks:
icpc -m64

Fortran benchmarks:
ifort -m64

Base Portability Flags

500.perlbench_r: -DSPEC_LP64 -DSPEC_LINUX_X64
502.gcc_r: -DSPEC_LP64
505.mcf_r: -DSPEC_LP64
520.omnetpp_r: -DSPEC_LP64
523.xalancbm_r: -DSPEC_LP64 -DSPEC_LINUX
525.x264_r: -DSPEC_LP64
531.deepsjeng_r: -DSPEC_LP64
541.leela_r: -DSPEC_LP64
548.exchange2_r: -DSPEC_LP64
557.xz_r: -DSPEC_LP64
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPEC CPU®2017 Integer Rate Result
Copyright 2017-2020 Standard Performance Evaluation Corporation

SPECrate®2017_int_base = 33.4
SPECrate®2017_int_peak = 34.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Base Optimization Flags
C benchmarks:
-`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
-`-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc`

C++ benchmarks:
-`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
-`-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/ -ljemalloc`

Fortran benchmarks:
-`-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div`
-`-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte`
-`-L/home/cpu2017/je5.0.1-64/ -ljemalloc`

Peak Compiler Invocation
C benchmarks (except as noted below):
-`icc -m64 -std=c11`

502.gcc_r: `icc -m32 -std=c11 -L/opt/intel/lib/ia32`

C++ benchmarks (except as noted below):
-`icpc -m64`

523.xalancbmk_r: `icpc -m32 -L/opt/intel/lib/ia32`

Fortran benchmarks:
-`ifort -m64`

Peak Portability Flags
500.perlbench_r: `-DSPEC_LP64 -DSPEC_LINUX_X64`
502.gcc_r: `-D_FILE_OFFSET_BITS=64`
505.mcf_r: `-DSPEC_LP64`
520.omnetpp_r: `-DSPEC_LP64`
523.xalancbmk_r: `-D_FILE_OFFSET_BITS=64 -DSPEC_LINUX`
525.x264_r: `-DSPEC_LP64`
531.deepsjeng_r: `-DSPEC_LP64`
541.leela_r: `-DSPEC_LP64`
548.exchange2_r: `-DSPEC_LP64`
557.xz_r: `-DSPEC_LP64`
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

SPECrater®2017_int_base = 33.4
SPECrater®2017_int_peak = 34.8

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

## Peak Optimization Flags

### C benchmarks:

500.perlbench_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-fno-strict-overflow -L/home/cpu2017/je5.0.1-64/
-1jemalloc

502.gcc_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-32/ -1jemalloc

505.mcf_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -L/home/cpu2017/je5.0.1-64/
-1jemalloc

525.x264_r: -Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -fno-alias
-L/home/cpu2017/je5.0.1-64/ -1jemalloc

557.xz_r: Same as 505.mcf_r

### C++ benchmarks:

520.omnetpp_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-64/ -1jemalloc

523.xalancbk_r: -Wl,-z,muldefs -prof-gen(pass 1) -prof-use(pass 2) -ipo
-xCORE-AVX512 -O3 -no-prec-div -qopt-mem-layout-trans=3
-L/home/cpu2017/je5.0.1-32/ -1jemalloc

531.deepsjeng_r: Same as 520.omnetpp_r

541.leela_r: Same as 520.omnetpp_r

### Fortran benchmarks:

-Wl,-z,muldefs -xCORE-AVX512 -ipo -O3 -no-prec-div
-qopt-mem-layout-trans=3 -nostandard-realloc-lhs -align array32byte
-L/home/cpu2017/je5.0.1-64/ -1jemalloc

The flags files that were used to format this result can be browsed at

# SPEC CPU®2017 Integer Rate Result

**Cisco Systems**

Cisco UCS C240 M5 (Intel Xeon Bronze 3104 1.70 GHz)

<table>
<thead>
<tr>
<th>SPECrate®2017_int_base = 33.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPECrate®2017_int_peak = 34.8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Test Date: Dec-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardware Availability: Aug-2017</td>
</tr>
<tr>
<td>Software Availability: Oct-2018</td>
</tr>
</tbody>
</table>

You can also download the XML flags sources by saving the following links:


 SPEC CPU and SPECrate are registered trademarks of the Standard Performance Evaluation Corporation. All other brand and product names appearing in this result are trademarks or registered trademarks of their respective holders.

For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

Tested with SPEC CPU®2017 v1.0.2 on 2018-12-13 11:12:20-0500.
Originally published on 2019-01-29.