Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5122 3.60 GHz)

**SPECspeed®2017_fp_base** = 55.9
**SPECspeed®2017_fp_peak** = Not Run

<table>
<thead>
<tr>
<th>Threads</th>
<th>SPECspeed®2017_fp_base (55.9)</th>
</tr>
</thead>
<tbody>
<tr>
<td>603.bwaves_s 8</td>
<td>53.2</td>
</tr>
<tr>
<td>607.cactuBSSN_s 8</td>
<td>45.0</td>
</tr>
<tr>
<td>619.lbm_s 8</td>
<td>60.7</td>
</tr>
<tr>
<td>621.wrf_s 8</td>
<td>28.4</td>
</tr>
<tr>
<td>627.cam4_s 8</td>
<td>45.5</td>
</tr>
<tr>
<td>628.pop2_s 8</td>
<td>34.3</td>
</tr>
<tr>
<td>638.imagick_s 8</td>
<td>59.3</td>
</tr>
<tr>
<td>644.nab_s 8</td>
<td>56.1</td>
</tr>
<tr>
<td>649.fotonik3d_s 8</td>
<td>53.3</td>
</tr>
</tbody>
</table>

**Hardware**

<table>
<thead>
<tr>
<th>CPU Name:</th>
<th>Intel Xeon Gold 5122</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max MHz:</td>
<td>3700</td>
</tr>
<tr>
<td>Nominal:</td>
<td>3600</td>
</tr>
<tr>
<td>Enabled:</td>
<td>8 cores, 2 chips</td>
</tr>
<tr>
<td>Orderable:</td>
<td>1,2 Chips</td>
</tr>
<tr>
<td>Cache L1:</td>
<td>32 KB I + 32 KB D on chip per core</td>
</tr>
<tr>
<td>L2:</td>
<td>1 MB I+D on chip per core</td>
</tr>
<tr>
<td>L3:</td>
<td>16.5 MB I+D on chip per chip</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
</tr>
<tr>
<td>Memory:</td>
<td>768 GB (24 x 32 GB 2Rx4 PC4-2666V-R)</td>
</tr>
<tr>
<td>Storage:</td>
<td>1 x 600G SAS 10K RPM</td>
</tr>
<tr>
<td>Other:</td>
<td>None</td>
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</table>

**Software**

<table>
<thead>
<tr>
<th>OS:</th>
<th>SUSE Linux Enterprise Server 12 SP2 (x86_64)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4.4.120-92.70-default</td>
</tr>
<tr>
<td>Compiler:</td>
<td>C/C++: Version 19.0.1.144 of Intel C/C++</td>
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<tr>
<td></td>
<td>Compiler for Linux;</td>
</tr>
<tr>
<td></td>
<td>Fortran: Version 19.0.1.144 of Intel Fortran Compiler for Linux</td>
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<tr>
<td>Parallel:</td>
<td>Yes</td>
</tr>
<tr>
<td>Firmware:</td>
<td>Version 4.0.1 released Oct-2018</td>
</tr>
<tr>
<td>File System:</td>
<td>xfs</td>
</tr>
<tr>
<td>System State:</td>
<td>Run level 3 (multi-user)</td>
</tr>
<tr>
<td>Base Pointers:</td>
<td>64-bit</td>
</tr>
<tr>
<td>Peak Pointers:</td>
<td>Not Applicable</td>
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<tr>
<td>Other:</td>
<td>None</td>
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<tr>
<td>Power Management:</td>
<td>--</td>
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</table>
## Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5122 3.60 GHz)

### SPEC CPU®2017 Floating Point Speed Result

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Threads</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
<th>Seconds</th>
<th>Ratio</th>
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</thead>
<tbody>
<tr>
<td>Base</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>603.bwaves_s</td>
<td>8</td>
<td>228</td>
<td>259</td>
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<td>259</td>
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<tr>
<td>607.cactuBSSN_s</td>
<td>8</td>
<td>313</td>
<td>53.2</td>
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<td>53.2</td>
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<td>53.1</td>
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<tr>
<td>619.lbm_s</td>
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<td>45.1</td>
<td>116</td>
<td>45.0</td>
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<tr>
<td>621.wrf_s</td>
<td>8</td>
<td>219</td>
<td>60.4</td>
<td>218</td>
<td>60.8</td>
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<td>60.7</td>
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<td>312</td>
<td>28.4</td>
<td>312</td>
<td>28.4</td>
<td>311</td>
<td>28.5</td>
</tr>
<tr>
<td>628.pop2_s</td>
<td>8</td>
<td>261</td>
<td>45.4</td>
<td>261</td>
<td>45.5</td>
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<tr>
<td>644.nab_s</td>
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<td>295</td>
<td>59.3</td>
<td>295</td>
<td>59.3</td>
<td>295</td>
<td>59.3</td>
</tr>
<tr>
<td>649.fotonik3d_s</td>
<td>8</td>
<td>162</td>
<td>56.3</td>
<td>164</td>
<td>55.7</td>
<td>162</td>
<td>56.1</td>
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<tr>
<td>654.roms_s</td>
<td>8</td>
<td>295</td>
<td>53.3</td>
<td>296</td>
<td>53.1</td>
<td>294</td>
<td>53.5</td>
</tr>
</tbody>
</table>

### SPECspeed®2017_fp_base = 55.9

### SPECspeed®2017_fp_peak = Not Run

Results appear in the order in which they were run. Bold underlined text indicates a median measurement.

### Operating System Notes
Stack size set to unlimited using "ulimit -s unlimited"

### General Notes

Environment variables set by runcpu before the start of the run:
- KMP_AFFINITY = "granularity=fine,compact"
- LD_LIBRARY_PATH = "/home/cpu2017/lib/ia32:/home/cpu2017/lib/intel64"
- OMP_STACKSIZE = "192M"

Binaries compiled on a system with 1x Intel Core i7-4790 CPU + 32GB RAM
memory using Redhat Enterprise Linux 7.4
Transparent Huge Pages enabled by default
Prior to runcpu invocation
Filesystem page cache synced and cleared with:

```
sync; echo 3>/proc/sys/vm/drop_caches
```

Yes: The test sponsor attests, as of date of publication, that CVE-2017-5754 (Meltdown) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5753 (Spectre variant 1) is mitigated in the system as tested and documented.
Yes: The test sponsor attests, as of date of publication, that CVE-2017-5715 (Spectre variant 2) is mitigated in the system as tested and documented.

### Platform Notes

BIOS Settings:
- Intel HyperThreading Technology set to Disabled
- CPU performance set to Enterprise

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5122 3.60 GHz)

SPECspeed®2017_fp_base = 55.9
SPECspeed®2017_fp_peak = Not Run

<table>
<thead>
<tr>
<th>CPU2017 License:</th>
<th>9019</th>
<th>Test Date:</th>
<th>Dec-2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Sponsor:</td>
<td>Cisco Systems</td>
<td>Hardware Availability:</td>
<td>Aug-2017</td>
</tr>
<tr>
<td>Tested by:</td>
<td>Cisco Systems</td>
<td>Software Availability:</td>
<td>Oct-2018</td>
</tr>
</tbody>
</table>

**Platform Notes (Continued)**

Power Performance Tuning set to OS Controls
SNC set to Disabled
Patrol Scrub set to Disabled
Sysinfo program /home/cpu2017/bin/sysinfo
Rev: r5797 of 2017-06-14 96c45e4568ad54c135fd618b0c091c0f
running on linux-dkz7 Mon Dec 10 06:14:51 2018

SUT (System Under Test) info as seen by some common utilities.
For more information on this section, see
[https://www.spec.org/cpu2017/Docs/config.html#sysinfo](https://www.spec.org/cpu2017/Docs/config.html#sysinfo)

From /proc/cpuinfo
model name : Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
  2 "physical id"s (chips)
  8 "processors"
cores, siblings (Caution: counting these is hw and system dependent. The following
excerpts from /proc/cpuinfo might not be reliable. Use with caution.)
cpu cores : 4
siblings : 4
physical 0: cores 0 5 9 13
physical 1: cores 3 4 6 7

From lscpu:
Architecture:          x86_64
CPU op-mode(s):        32-bit, 64-bit
Byte Order:            Little Endian
CPU(s):                8
On-line CPU(s) list:   0-7
Thread(s) per core:    1
Core(s) per socket:    4
Socket(s):             2
NUMA node(s):          2
Vendor ID:             GenuineIntel
CPU family:            6
Model:                 85
Model name:            Intel(R) Xeon(R) Gold 5122 CPU @ 3.60GHz
Stepping:              4
CPU MHz:               2775.355
CPU max MHz:           3700.0000
CPU min MHz:           1200.0000
BogoMIPS:              7183.11
Virtualization:        VT-x
L1d cache:             32K
L1i cache:             32K
L2 cache:              1024K
L3 cache:              16896K
NUMA node0 CPU(s):     0-3

(Continued on next page)
Cisco Systems  
Cisco UCS C240 M5 (Intel Xeon Gold 5122 3.60 GHz)  

**SPEC CPU®2017 Floating Point Speed Result**  

**Copyright 2017-2020 Standard Performance Evaluation Corporation**  

---

**SPECspeed®2017_fp_base = 55.9**  
**SPECspeed®2017_fp_peak = Not Run**  

---

**CPU2017 License:** 9019  
**Test Sponsor:** Cisco Systems  
**Tested by:** Cisco Systems  
**Test Date:** Dec-2018  
**Hardware Availability:** Aug-2017  
**Software Availability:** Oct-2018  

**Platform Notes (Continued)**

NUMA node1 CPU(s): 4-7

Flags: fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov
pat pse36 clflush dts acpi mmx fxsr sse sse2 ss ht tm pbe syscall nx pdpe1gb rdtscp
lm constant_tsc arch_perfmon pebs bts rep_good nopl xtopology nonstop_tsc
aperfmperf eagerfpu pni pclmulqdq dtes64 monitor ds_cpl vmx smx est tm2 ssse3 sdbg
fma cx16 xtral pdcm pclid dca sse4_1 sse4_2 x2apic movbe popcnt tsc_deadline_timer aes
xsave avx f16c rdrand lahf_lm abm 3dnowprefetch ida arat epb invpcid_single pln pts
dtherm hwp hwcap_window hwcap_epp hwp_kpg req intel_pt rsb_ctxts spec_ctrl stibp
repoline kaiser tpr_shadow vmmvx flexpriority ept vpid fsgsbase tsc_adjust bmi1 hle
avx2 smep bmi2 erms invpcid rtm cqm mpx avx512f avx512dq rdseed adx smap clflushopt
c1wb avx512cd avx512bw avx512vl xsaveopt xsaves xgetbv1 cqm_llc cqm_occuc_llc

From numactl --hardware WARNING: a numactl 'node' might or might not correspond to a
physical chip.

available: 2 nodes (0-1)
  node 0 cpus: 0 1 2 3
  node 0 size: 385626 MB
  node 0 free: 381638 MB
  node 1 cpus: 4 5 6 7
  node 1 size: 387054 MB
  node 1 free: 383100 MB
  node distances:
    node   0   1
    0:  10  21
    1:  21  10

From /proc/meminfo

  MemTotal:       791225660 kB
  HugePages_Total:       0
  Hugepagesize:       2048 kB

From /etc/*release* /etc/*version*

  SuSE-release:
    SUSE Linux Enterprise Server 12 (x86_64)
    VERSION = 12
    PATCHLEVEL = 2
    # This file is deprecated and will be removed in a future service pack or release.
    # Please check /etc/os-release for details about this release.
  os-release:
    NAME="SLES"
    VERSION="12-SP2"
    VERSION_ID="12.2"
    PRETTY_NAME="SUSE Linux Enterprise Server 12 SP2"
    ID="sles"

(Continued on next page)
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5122 3.60 GHz)

SPECspeed®2017_fp_base = 55.9
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Tested by: Cisco Systems

Test Date: Dec-2018
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Platform Notes (Continued)

```
ANSI_COLOR="0;32"
CPE_NAME="cpe:/o:suse:sles:12:sp2"

uname -a:
    Linux linux-dkz7 4.4.120-92.70-default #1 SMP Wed Mar 14 15:59:43 UTC 2018 (52a83de)
    x86_64 x86_64 x86_64 GNU/Linux

run-level 3 Dec 10 00:50

SPEC is set to: /home/cpu2017

Filesystem     Type  Size  Used Avail Use% Mounted on
/dev/sda2      xfs   500G  124G  377G  25% /

Additional information from dmidecode follows. WARNING: Use caution when you interpret this section. The 'dmidecode' program reads system data which is "intended to allow hardware to be accurately determined", but the intent may not be met, as there are frequent changes to hardware, firmware, and the "DMTF SMBIOS" standard.

BIOS Cisco Systems, Inc. C240M5.4.0.1.139.1003182220 10/03/2018

Memory:
    12x 0xCE00 M393A4K40BB2-CTD 32 GB 2 rank 2666
    12x 0xCE00 M393A4K40CB2-CTD 32 GB 2 rank 2666

(End of data from sysinfo program)
```

Compiler Version Notes

```
C               | 619.lbm_s(base) 638.imagick_s(base) 644.nab_s(base)
------------------------------------------------------------------------------
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

C++, C, Fortran | 607.cactuBSSN_s(base)
------------------------------------------------------------------------------
icpc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
icc (ICC) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.
------------------------------------------------------------------------------

Fortran         | 603.bwaves_s(base) 649.fotonik3d_s(base) 654.roms_s(base)
(Continued on next page)
```
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5122 3.60 GHz)

SPECSpeed®2017_fp_base = 55.9
SPECSpeed®2017_fp_peak = Not Run

Compiler Version Notes (Continued)

ifort (IFORT) 19.0.1.144 20181018
Copyright (C) 1985-2018 Intel Corporation. All rights reserved.

---------------------------------------------------------------
Fortran, C | 621.wrf_s(base) 627.cam4_s(base) 628.pop2_s(base)
---------------------------------------------------------------

Base Compiler Invocation

C benchmarks:
icc -m64 -std=c11

Fortran benchmarks:
ifort -m64

Benchmarks using both Fortran and C:
ifort -m64 icc -m64 -std=c11

Benchmarks using Fortran, C, and C++:
icpc -m64 icc -m64 -std=c11 ifort -m64

Base Portability Flags

603.bwaves_s: -DSPEC_LP64
607.cactusBSSN_s: -DSPEC_LP64
619.lbm_s: -DSPEC_LP64
621.wrf_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
627.cam4_s: -DSPEC_LP64 -DSPEC_CASE_FLAG
628.pop2_s: -DSPEC_LP64 -DSPEC_CASE_FLAG -convert big_endian
-assume byterecl
638.imagick_s: -DSPEC_LP64
644.nab_s: -DSPEC_LP64
649.fotonik3d_s: -DSPEC_LP64
654.roms_s: -DSPEC_LP64
Cisco Systems
Cisco UCS C240 M5 (Intel Xeon Gold 5122
3.60 GHz)

SPECspeed®2017_fp_base = 55.9
SPECspeed®2017_fp_peak = Not Run

CPU2017 License: 9019
Test Sponsor: Cisco Systems
Test Date: Dec-2018
Tested by: Cisco Systems
Hardware Availability: Aug-2017
Software Availability: Oct-2018

Base Optimization Flags

C benchmarks:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP

Fortran benchmarks:
-DSPEC_OPENMP -xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp
-nostandard-realloc-lhs -align array32byte

Benchmarks using both Fortran and C:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

Benchmarks using Fortran, C, and C++:
-xCORE-AVX512 -ipo -O3 -no-prec-div -qopt-prefetch
-ffinite-math-only -qopt-mem-layout-trans=3 -qopenmp -DSPEC_OPENMP
-nostandard-realloc-lhs -align array32byte

The flags files that were used to format this result can be browsed at

You can also download the XML flags sources by saving the following links:
http://www.spec.org/cpu2017/flags/Intel-ic19.0-official-linux64.xml
http://www.spec.org/cpu2017/flags/Cisco-Platform-Settings-V1.2-revH.xml

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For questions about this result, please contact the tester. For other inquiries, please contact info@spec.org.

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